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Monolithically Integrated GaN Gate Drivers–A Design Guide

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ABSTRACT In recent years, an increasing trend towards GaN integration can be observed, enabled by the lateral structure of the GaN technology. A key improvement over a discrete implementation is the integration of a monolithic gate driver. This tutorial-style article aims to give insight into the design flow. It starts with the possibilities of GaN technologies in terms of IC design followed by basic driving principles of GaN HEMTs. Gate loop requirements and recommendations for the gate driver output stage are explained. A flowchart for the design of integrated gate drivers is presented with the boundary constraints from the technology, topology research, and selection using a step-by-step guide. The design flow is run through with an example scenario and the realized gate driver design is optimized for low power consumption and fast switching, which is verified with simulations and measurements. Thus, a guide is given for the design of a monolithically integrated GaN gate driver to further advance, promote, and accelerate integration in GaN.

INDEX TERMS Gallium nitride, power integrated circuits, monolithic integrated circuits, driver circuits, gate drivers.

I. INTRODUCTION

Gate drivers provide the link between the controller and the power semiconductor transistor. The logic input signal of the gate driver is typically a pulse-width modulated (PWM) signal from digital signal processors (DSPs), microcontrollers (MCUs), or application-specific integrated circuits (ASICs) with supply voltages of 3.3–5 V. This input signal is adapted by the gate driver to the switchable power transistors such as Si-based MOSFETs and IGBTs, SiC MOSFETs, but also GaN HEMTs, each introducing specific requirements for the gate driver circuit such as turn-on voltages of 5–20 V and gate currents of 0.1–10 A [1], [2].

One of the fastest-growing classes of power transistors is the GaN HEMT due to its superior figure-of-merits ($R_{ON} \cdot A$ [3] and $R_{ON} \cdot Q$ [4]) for highly efficient and highly compact switching converters in power electronics [5], [6], [7]. Today's commercially available GaN transistors are mostly manufactured in a GaN-on-Si technology with cost-effective and large-scale Si substrates [8]. Based on the two-dimensional electron gas (2DEG) [9], the lateral structure enables the integration of multiple devices on the same die. This is a unique advantage over alternative power technologies such as vertical SiC. Thus, additional functional blocks of the power converter can be integrated into the GaN-on-Si power IC technology [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], which are conventionally designed in a comparable lateral technology such as Si BCD. This so-called GaN power integration has become a technology trend in power electronics, pushed for years by Academia [22] and finally transferred into commercial products by industry and numerous companies like Efficient Power Conversion (EPC), GaN Systems, Navitas Semiconductor, and Innoscience, foundries like TSMC and IMEC, as well as start-ups like Wise-Integration, GaN-Power International, and Cambridge GaN Devices (CGD) [8].

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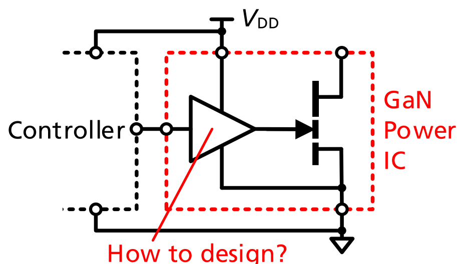

FIGURE 1. Monolithically integrated gate driver with GaN HEMT, resulting in a GaN power IC.

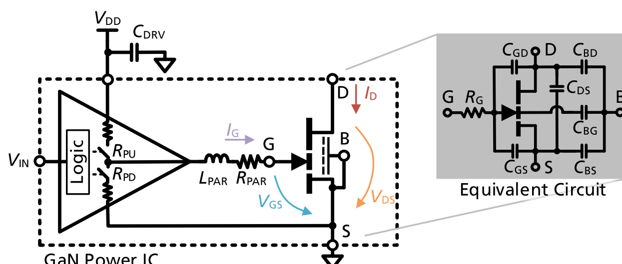

FIGURE 2. Schematic of a GaN HEMT driving adapted from [24] with equivalent circuit consisting of 4-terminal capacitances [33], [34] and internal gate resistor R_G.

GaN power ICs consisting of a GaN power HEMT and an integrated gate driver (as shown in Fig. 1) are naturally the first step of monolithic GaN integration. They minimize the parasitic gate loop inductance [23], thereby reducing critical ringing and associated overvoltage stress. This enables high-switching frequencies with steep high-voltage transients. There are already many integrated GaN gate drivers with different topologies and optionally voltage supply generation (see Section IV-A). To further advance integration [19], additional functional blocks can be integrated on the same die alongside the power HEMT and driver, enabling ultra-compact high-efficiency power converter systems. This includes but is not limited to sensing and protection circuits. However, there is no comprehensive design methodology for integrated GaN gate drivers available, yet. This article, therefore, aims to answer the question: How to design an integrated GaN gate driver depending on different optimization goals, technological possibilities, and boundary conditions while fulfilling the application-specific requirements (visualized in Fig. 1)? Based on different GaN gate driver topologies, guidelines for designs are presented for non-isolated and voltage-source controlled gate drivers for normally-off GaN transistors [24].

The article is organized as follows. Section II gives an overview of the technological possibilities of integrating monolithic GaN circuits. In Section III the driving mechanism of GaN HEMTs and in connection some specifications of the gate driver are discussed. Section IV presents the GaN gate driver design based on a design flow. This requires topology research to give a step-by-step guide for the topology selection. The design flow is demonstrated using an example process resulting in an optimized design. Section V concludes the article.

II. GAN TECHNOLOGIES

Depending on the choice of GaN technology or process, there are differences in design possibilities. A typical substrate for a GaN technology is a Si wafer due to its low cost and availability in large diameters [8]. Besides GaN-on-Si, other substrates can be used. Processing monolithic GaN circuits on isolated substrates such as Si-on-insulator (SOI) [25], or ceramic substrates e.g., from Qromis (QST) [26] allows to isolate different voltage domains on-chip and suppress the backgating effect [27]. A widely used substrate is sapphire (Al_2O_3) [8], which also has insulating properties. Based on its inherent structure, the GaN HEMT is historically a depletion-mode (d-mode) device [28]. Normally-off GaN HEMTs can be manufactured with an additional p-GaN layer at the gate, shifting the negative threshold of the inherently d-mode device to a positive voltage resulting in an e-mode type device. This behavior is favorable to ensure inherent fail-safe operation of the power transistors. In commercial technologies, depending on the gate module, either only d-mode, only e-mode, or both HEMT types are available. This is decisive for the gate driver design and especially the topology selection. GaN HEMTs can be designed in different voltage classes, ranging from 12 V to 650 V or partly even up to 1200 V [8]. Besides low-voltage HEMTs, rectifiers are desirable for the design of monolithic ICs. Different rectifier concepts can be realized. Whereas some technologies offer low forward drop Schottky barrier diodes (SBDs), it is possible to implement lateral field-effect rectifiers (LFERs) utilizing diode-configured e-mode devices [29]. The LFER's turn-on voltage can be adjusted by changing its length [30] but it is typically higher compared to the SBD. It is also possible to integrate passive components such as resistors, capacitors, and spiral inductors. Their availability and characteristics can vary strongly with the used technology platform. Stacked MIM capacitors can achieve capacitance densities of 0.3 fF/μm^2 [25], which can even be enhanced up to 1.2 fF/μm^2 by adding the 2DEG as an additional virtual metal layer to the capacitor stack [19]. Equivalent to the MOS capacitor in Si-based technologies, the p-GaN gate capacitor exists in GaN technology with capacitance densities of 1.2 fF/μm^2 [19] to $>$1.7 fF/μm^2 [31] but featuring a limited operating voltage range from V_{TH} to the max. V_{GS}. P-type devices based on a two-dimensional hole gas are typically not available in most GaN technologies. Even though physically feasible [32], they are not practically usable for circuit design due to the low hole mobility. Thus, CMOS logic cannot be realized, challenging the gate driver design.

III. DRIVING GAN HEMTS

The main purpose of the gate driver is to safely turn the GaN HEMT on and off while aiming for maximum switching speed. Fig. 2 schematically shows a voltage-source controlled gate driver connected to a GaN HEMT adapted from [24],

TABLE 1 Comparison of Three Exemplary Commercial GaN HEMTs

GaN HEMTs	EPC2218 (100 V, 60 A) [37]	GS0650182L (650 V, 18 A) [38]	IGLD60R190D1 (600 V, 10 A) [39]
Technology	p-GaN	p-GaN	GIT
C_{ISS} (C_{GD}+C_{GS})	1189 pF	132 pF	157 pF
C_{RSS} (C_{GD})	4.3 pF	0.4 pF	0.15 pF
Q_G	10.5 nC	4.0 nC	3.2 nC
R_G	0.4 Ω	1.3 Ω	0.74 Ω
V_{TH} (min./typ.)	0.8/1.1 V	1.1./1.7 V	0.9/1.2 V
V_{DD} typ.	5 V	6 V	3 V
V_{GS} ratings	-4…6 V	-10…7 V	-10
$R_{DS(ON)}$	2.4 mΩ	78 mΩ	140 mΩ
FOM ($R_{DS(ON)}$×Q_G)	0.025 ΩnC	0.312 ΩnC	0.448 ΩnC

which is a commonly used gate driver type. Fig. 2 also depicts the equivalent switching capacitance of the 4-terminal power HEMT device (C_{GD}, C_{GS}, C_{DS}, C_{BG}, C_{BD}, C_{BS}) [33], [34] and the internal gate resistance R_G, which are relevant for the switching behavior [35], [36]. In the scope of this work, the backgating effect is not considered because the backgate is usually short-circuited to the source terminal (see Fig. 2).

Together with additional parasitic inductance L_{PAR} and resistance R_{PAR} (bond wires, tracks, and traces), the switch transistor capacitances form an *RLC* resonant tank – known as the gate loop. In an underdamped loop, fast gate drivers have the risk of oscillation. Addressing this, additional external gate resistors $R_{G,EXT}$ are typically placed in discrete configurations to slow down the drivers, damp the oscillations, and keep the limits of the min./max. gate-source voltage. Monolithically integrating the driver circuit together with the GaN HEMT can significantly reduce the gate loop inductance by eliminating bond wires, packaging tracks, and PCB traces between driver and GaN HEMT. This enables significantly lower loop resistance and thus faster drivers. Sufficient damping of the remaining loop can then be ensured by the driver design (see Section A).

In Fig. 2 the driver output stage is modeled as resistors. To turn on the power switch, the power HEMT gate is pulled up to V_{DD} via $R_{PU,}$ which represents the pull-up resistance of the gate driver's output stage. The supply voltage V_{DD} of the driver must therefore be significantly higher than the threshold voltage of the power transistor (also called overdrive), to ensure strong turn-on and low on-resistance of the GaN power switch. However, some safety margin between max. gate-source voltage and V_{DD} is recommended. For turn-off, the power HEMT gate is connected to the source terminal via the driver's pull-down resistance R_{PD}. The requirements for the turn-on and turn-off gate loop of standard normally-off HEMTs with integrated gate driver are described below.

Table 1 lists the most important parameters and ratings of three exemplary GaN HEMTs from three different manufacturers [37], [38], [39]. The gate charge of GaN HEMTs is by a factor of ∼10 smaller compared to Si MOSFETs with corresponding specifications resulting from inherently lower parasitic capacitances [24]. Normally-off GaN HEMTs

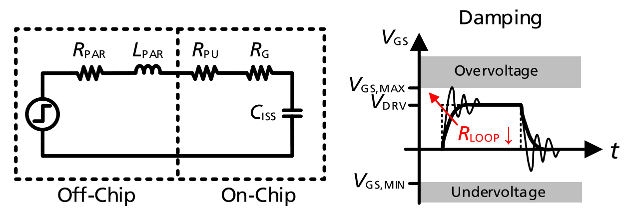

FIGURE 3. (Left) Turn-on gate loop consisting of parasitic components forming an *RLC* resonant circuit and (right) influence of damping on the gate-source voltage V_{GS} with the corresponding limits.

commonly have a p-GaN gate structure [40]. Depending on the metal-p-GaN contact in the technology, the gate can have a higher (referred to as ohmic) or lower (Schottky) leakage current [41]. The gate injection transistor (GIT) has an ohmic metal-p-GaN contact with additional recess, which makes the technological process more complex. Additionally, the GIT requires a current-source controlled gate driver or voltage-source controlled, either with special gate resistor network consisting of an *RC* interface [42] or new circuit approaches [43], and is not further discussed in this article. The approaches presented in the following can be applied to GaN HEMTs with a p-GaN gate structure, either if it is ohmic- or Schottky-type. There are some charge trapping processes in GaN transistors that can lead to effects such as dynamic $R_{DS(ON)}$ increase or threshold voltage instabilities [41]. These effects require consideration in the gate driver design and especially in the gate loop.

A. REQUIREMENTS FOR POWER HEMT TURN-ON

Fig. 3 shows the turn-on gate loop consisting of the loop resistance $R_{LOOP} = R_{PU} + R_{PAR} + R_G$, parasitic inductance L_{PAR} and the input capacitance of the GaN power HEMT C_{ISS}. Placing an on-chip capacitor for supply decoupling can significantly complicate the considerations regarding gate loop damping. The stronger the gate driver, the faster the transition from off to on or vice versa, and the lower the hard-switching losses. It is thus desirable to keep the total loop resistance as low as possible. Based on the application, there can furthermore be a specification for a maximum rise time of the power HEMT gate voltage. From this, a maximum loop resistance can be derived, e.g., by assuming a simple RC-delay in the gate loop. However, the risk of oscillations or overvoltage and undervoltage of the gate-source voltage increases when an underdamped parasitic RLC resonant tank is formed in the gate loop. The damping is determined by the loop resistance, directly affecting the overshoot- and ringing behavior. While R_{PAR} and R_G depend on the wiring and layout R_{PU} can be set by the gate driver design and in particular the output stage (see Section D). To achieve critical damping and thereby suppress any oscillations R_{PU} can be calculated as follows [44], [45], [46]

$$R_{PU,\ OPT} = 2 \cdot \sqrt{\frac{L_{PAR}}{C_{ISS}}} - R_{PAR} - R_G. \tag{1}$$

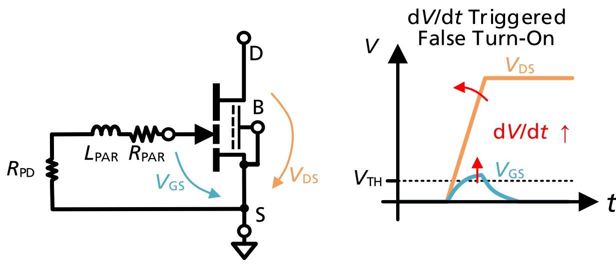

FIGURE 4. (Left) Turn-off gate loop and (right) dV/dt triggered false turn-on.

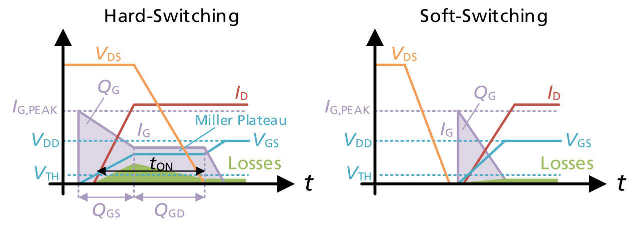

FIGURE 5. Switching curves (drain-source voltage V_{DS}, drain current I_D, gate-source voltage V_{GS}, gate current I_G, and resulting losses) of the turn-on transition in (left) hard- and (soft) soft-switching operation adapted from [24], [48].

Thereby, the parasitic inductance L_{PAR} mainly results from the connection to the gate supply bypass capacitance C_{DRV} (see Fig. 2) through the SMD package of the capacitor, the connection of the PCB, and possible bond wires to the GaN power IC. An example value for the realization of the GaN IC in a QFN package is $L_{PAR} = 2.5$ nH [24]. Exemplary gate loop inductance values are described in [24]. A more dynamic approach resulting in a possibly smaller loop resistance is to design the loop allowing oscillations but designing the resistance to limit the overshoot to the maximum gate-source voltage. R_{PU} can then be calculated as follows [46]

$$R_{PU,\,MIN} = 2 \cdot \frac{2\,V_{DRV} - V_{GS,MAX}}{V_{DRV}} \cdot \sqrt{\frac{L_{PAR}}{C_{ISS}}} - R_{PAR} - R_G. \tag{2}$$

Choosing R_{PU} in between the boundaries given by (1) and (2), i.e., $R_{PU,MIN} \leq R_{PU} \leq R_{PU,OPT}$ ensures to meet the requirements for a safe turn-on while preventing overvoltage stress to the power HEMT gate.

B. REQUIREMENTS FOR THE TURN-OFF GATE LOOP

Fig. 4 shows the turn-off gate loop with the pull-down resistor R_{PD} of the integrated gate driver. In the monolithic implementation, the parasitic inductance in the turn-off loop is formed only by on-chip connections and is thus negligibly small. During switching transients, the drain of the power HEMT experiences high dV/dt, thereby the gate-to-drain capacitance of the power HEMT (see C_{GD} in Fig. 2) is charged through the gate driver. The current then flowing through $R_{LOOP} = R_{PD} + R_{PAR} + R_G$ causes a voltage drop: $V = C_{GD} \cdot \mathrm{d}V/\mathrm{d}t \cdot R_{LOOP}$. If this exceeds the threshold voltage, the GaN HEMT is unintentionally turned-on, which is called dV/dt triggered turn-on. To prevent this, the driver should be designed strong enough to keep the power HEMT in off-state. The smaller R_{PD}, the higher the protection against dV/dt triggered false turn-on, as shown in Fig. 4. The respective max. R_{PD} can be calculated as follows [44]

$$R_{PD,MAX} = \frac{V_{TH,MIN} + 0.004\ \mathrm{V}/^{\circ}\mathrm{C} \cdot \left(T_{J,MAX} - 25^{\circ}C\right)}{C_{RSS} \cdot \frac{\mathrm{d}V_{DS}}{\mathrm{d}t}} - R_{PAR} - R_G, \tag{3}$$

where $V_{TH,MIN}$ is the min. gate threshold voltage at 25°C, 0.004 V/°C being a suitable approximation for the temperature coefficient of V_{TH} [47], $T_{J,MAX}$ is the max. junction temperature and dV_{DS}/dt is the application-specific drain-source slew rate. The on-state resistance of an e-mode GaN HEMT has a proportional-to-absolute-temperature (PTAT) behavior. Thus, $R_{PD} \leq R_{PD,MAX}$ should be ensured over the aspired temperature range to meet the requirements for a safe off-state.

C. DRIVER LOSSES

The losses that are directly linked to the gate driver are gate charge losses P_G, driver power dissipation P_{DRV}, and the hard-switching losses P_{SW}. Fig. 5 shows the switching curves of a turn-on transition in hard- and soft-switching operation adapted from [24], [48]. The gate charge losses (CV^2-losses) occur during charging and discharging of the input capacitance of the HEMT C_{ISS}. The gate current is provided by the gate driver. The average value of the gate current $I_{G,AV}$ corresponds to the gate charge Q_G multiplied by the switching frequency f_{sw}. This allows to calculate the gate charge losses as follows [44], [49]

$$P_G = Q_G \cdot f_{SW} \cdot V_{DD} = C_{ISS} \cdot f_{SW} \cdot V_{DD}^2. \tag{4}$$

The switching frequency and supply voltage are often specified by the application. The power losses to drive the gate P_{DRV} of the power HEMT are dissipated in the gate driver circuit. The dissipating components can be identified as the combination of series ohmic impedances in the gate drive path and the power loss can be calculated as [44]

$$P_{DRV} = \frac{1}{2} \cdot Q_G \cdot f_{SW} \cdot V_{DD} \cdot \sum_{i \in \{R_{PU}, R_{PD}\}} \frac{i}{i + R_{PAR} + R_G}. \tag{5}$$

One way to reduce the power losses when driving the gate is to use a resonant gate driver that charges the gate via an inductor. This inductor can be added to the parasitic inductance L_{PAR} in the gate loop. The oscillations, suppressed by the R_{PU} design in Section III-A, are favored in this case and even utilized, requiring an underdamped loop. Despite the theoretically achievable maximum efficiency of 100% with resonant drivers [24] physical implementations have shown

TABLE 2 Recommendations for the Gate Driver Output Stage

	R_{PU}	R_{PD}	R_{PU}/R_{PD}
Hard-Switching	$\geq R_{PU,MIN}$ $\leq R_{PU,OPT}$	$\leq R_{PD,MAX}$	≤ 1
Soft-Switching		$\leq R_{PD,MAX}$	~ 1

to not accomplish this [49] and typically even perform worse than non-resonant implementations.

In the hard-switching case, the switching energies can be approximated from the area of the triangle indicated in Fig. 5 from the overlap of the application-specific drain current I_D and drain-source voltage V_{DS} during turn-on time t_{ON} and, at the turn-off transition, during the turn-off time t_{OFF}. The switching losses, in turn, result from the switching energies multiplied by the switching frequency [44],

$$P_{SW} = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot (t_{ON} + t_{OFF}) \cdot f_{SW}. \quad (6)$$

A more accurate approximation of t_{ON}/t_{OFF} can be found in [44].

D. THE GATE DRIVER OUTPUT STAGE

From Section III-A and III-B recommendations for the output stage of the driver consisting of R_{PU} and R_{PD} can be given in the hard-switching case. Note that the ratio R_{PU}/R_{PD} should be ≤ 1 because C_{ISS} (see Fig. 2 and Table 1) is a V_{DS}-dependent capacitance and is smaller in off-state at high V_{DS}. In the soft-switching case, however, this is different. R_{PD} can be calculated according to formulas (1) and (2) to minimize the delay and dead time. In addition, $R_{PD,MAX}$ must not be exceeded according to formula (3) to avoid a dV/dt triggered false turn-on. R_{PU} is not critical because the drain voltage transient has already happened before the transistor is turned on (see Fig. 5) and can be chosen equal to R_{PD} [48]. A good trade-off can be $R_{PU} = R_{PD}$ for hard- and soft-switching applications. The recommendations are listed in Table 2.

Furthermore, to protect other on-chip circuits from the steep gate loop-related transients, it can be beneficial to provide a separate supply pin for the final driver stage.

IV. GAN GATE DRIVER DESIGN

Various integrated GaN gate drivers have been presented in the literature. These designs often include additional functions, summarized in Fig. 6, such as dV/dt-control [30], [50], [51], supply regulator (also bootstrap circuitry) [52], [53], [54], input logic (standby-circuitry, Schmitt trigger, level shifter) [13], [55], [56]. Also, protection functions like an under-voltage lockout, over-temperature protection, and over-current protection (UVLO, OTP, OCP) may be included [47], [57], [58]. This work's focus lies on the design of a monolithic GaN gate driver stage (marked by the box in the lower right of Fig. 6). Therefore, a design flow is introduced in Fig. 7. It starts with the input data of the application, power HEMT design, constraints, and design goals. For the gate driver topology selection, the available devices in the GaN technology

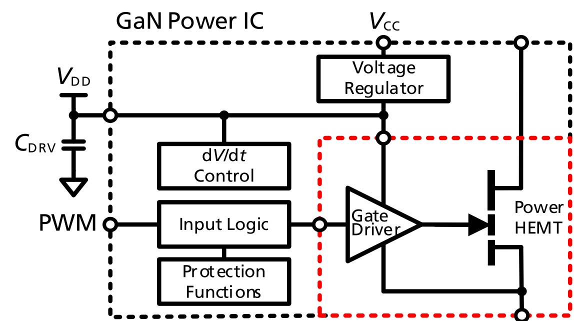

FIGURE 6. GaN power IC consisting of GaN power HEMT, gate driver and further functions, such as dV/dt-control, regulator (also bootstrap circuitry), input logic (standby-circuitry, Schmitt trigger, level shifter), and protection functions (UVLO, OTP, OCP).

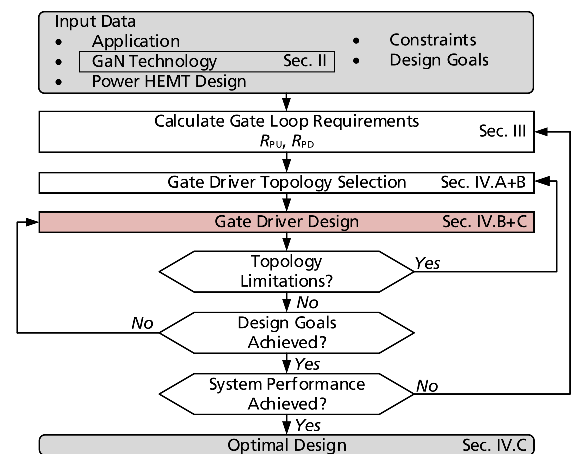

FIGURE 7. Flowchart of the proposed integrated GaN gate driver design flow.

are essential, which is why GaN technologies are discussed in detail in Section II. The next step is the calculation of the gate loop requirements with R_{PU} and R_{PD} (see Section III.). With the topology research background, a step-by-step guide for the topology selection and design is given. Different topology discussions are considered and evaluated based on various GaN technologies, criteria, and boundary conditions. Finally, the design flow is run through using a practical example for an application scenario, resulting in an optimized GaN gate driver.

A. TOPOLOGY RESEARCH

Due to the lack of p-type devices, alternative implementations are required to realize logic and also gate driver circuits. These can be direct n-type logic circuits (NMOS) also called direct coupled FET logic (DCFL, for technologies w/ d-mode HEMTs) or resistor-transistor logic (RTL, for technologies w/o d-mode HEMTs). Fig. 8 shows a DCFL and RTL inverter. Other versions of such simple inverters include bootstrapping [59], [60] or comprise a combination of resistor and d-mode HEMT [19]. Another alternative is to address the lack of complementary p-type devices with complementary signals to mimic CMOS behavior, resulting in pseudo-complementary

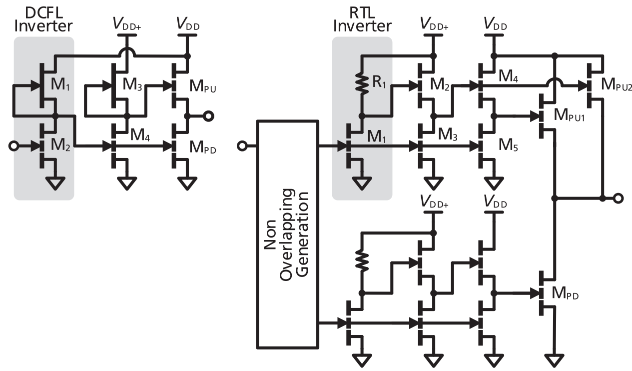

FIGURE 8. **(Left) Single [52], [60], [63], [64] and (right) split [13] path gate driver topology.**

FET logic (PCFL) [61], however, mainly suitable for technologies with low threshold voltage of e-mode GaN HEMTs e.g., <1 V.

A straightforward approach to forming a gate driver is to implement a string of simple inverters in a tapered manner as it is common with CMOS inverters [62]. Without p-type devices, this leads to high static current losses (V_{DD}/R_{PU}) in the DCFL and RTL inverters, especially in the final stage, where the R_{PU} can be in a range of only a few ohms. A typical driver output stage consists of two n-type e-mode devices realizing R_{PU} (see Section III-A) by a pull-up device (M_{PU}) and R_{PD} (see Section III-B) by a pull-down device (M_{PD}) with their on-state resistances $R_{DS,ON}$. M_{PU} and M_{PD} can be part of a split-path or single-path topology driver. Each path can then be formed either by a single stage or a multi-stage. Thereafter, each stage can be built by combining simple inverters and push-pull buffer stages. Completing the driver topology, a rail-to-rail driving concept has to be found.

An overview of two exemplary implementations with single [52], [60], [63], [64] and split path [13] presented in the literature is illustrated in Fig. 8. There are different concepts to realize the increased supply voltage V_{DD+} and thus a rail-to-rail driving: two supply voltages [63], bootstrapping [52], or charge pump [13], [60], [64]. These comprise propagation delays in a range from 1.7 ns [63] to 50 ns [13], [23] and a wide range of static power consumption. Clearly, different design goals were focused. Hence, the variation in reported performance results in a lack of comparability.

B. STEP-BY-STEP GUIDE

In the following a methodological approach to building topologies applicable in a monolithic GaN technology is presented according to the recommended topology selection steps as presented in Fig. 9. The choice of implementation depends on the technological possibilities. Table 3 gives an additional guide for the driver topology decision steps listing advantages of the different implementation options.

Step 1: The first decision in the topology selection is usually to choose a single or split path implementation. In a single path topology [64] M_{PU} and M_{PD} are controlled together.

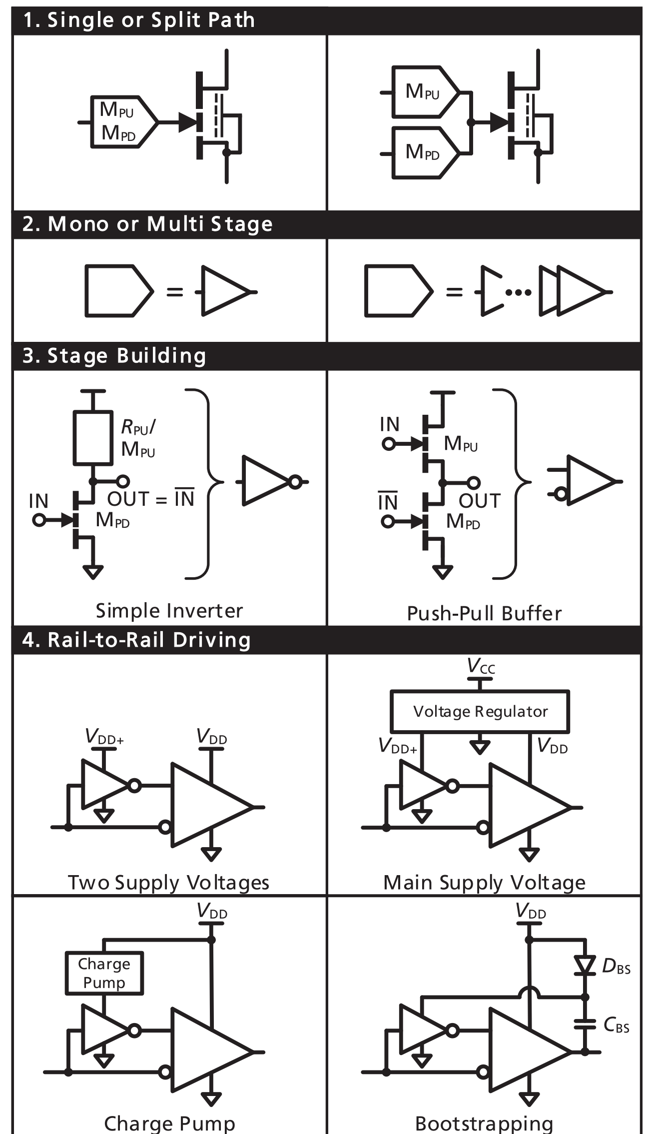

FIGURE 9. **Step-by-step guide of the topology selection.**

Cross-conduction can then occur in the final driver stage if the pull-up and pull-down device are turned on simultaneously even for a short amount of time. This causes unwanted power losses in the gate driver. Controlling M_{PU} and M_{PD} individually in a split path manner can suppress this. The separate control paths allow to prevent overlapping on-states of M_{PU} and M_{PD}, which can be achieved by either introducing asymmetrical timing in the two paths, called Skewing [65], or by providing non-overlapping signals to the split up path e.g., [13]. The decision for a split path can be based on the overall power consumption requirements limiting the allowable cross-conduction and also on the timing budget. A split path with a non-overlap generation logic circuit can however introduce additional propagation delay.

Step 2: Select a mono-stage or a multi-stage approach. Either the power HEMT directly or the separate pull-up and

pull-down device can be operated by a mono-stage [66] or a string of stages (multi-stage) [50]. In a mono-stage implementation, the input signal is applied to all elements in the stage, whereas in a multi-stage built, the signal is decomposed by two or more subsequent stages. The use of multiple stages allows for a tapering of the stage size, thereby allowing for a small input capacitance while accepting low drive strength at the first stage and enabling strong driving power in the last. However, multiple subsequent stages affect the propagation delay of the driver circuit. The built of the stage can thereby be relevant for making this discussion. It is hence, discussed in the following.

Step 3: A mono-stage can be a simple inverter whereas a string of inverters forms a multi-stage circuit. In a monolithic GaN technology, each stage can be formed by combining simple inverters together with push-pull buffers. Utilizing the simple inverter results in a trade-off between switching speed and static power consumption, both determined by the pull-up resistance R_{PU} ($P \approx T_{LOW} \cdot f\mathrm{sw} \cdot V_{DD}^2/R_{PU}$). Furthermore, it shows asymmetrical output slopes defined by the ratio of pull-up resistance to on-state resistance of the pull-down device: $R_{PU}/R_{ON,MPD}$ [45]. This ratio also affects the output low-state of the inverter: $V_{OUT,LOW} = R_{ON,MPD}/(R_{PU}+R_{ON,MPD}) \cdot V_{DD}$. The benefits of the simple inverter are that it requires only one input signal and provides a full-rail output high state: $V_{OUT,HIGH} = V_{DD}$. A push-pull buffer consists of two n-type e-mode devices operated by complementary signals. Such a buffer stage requires that both the input signal IN and additionally its logical inverse $\overline{IN}$ are available. $\overline{IN}$ can be provided by a simple inverter. By ensuring that either device is always turned off the static power consumption of the push-pull buffer is significantly lower compared to the simple inverter. Moreover, symmetrical slopes at the output can be achieved. The cascading possibility of push-pull buffers is limited. Due to the source follower behavior of the pull-up device, the steady output high state of a push-pull buffer can be limited depending on the voltage level of the input signal

$$V_{OUT,HIGH} = \begin{cases} V_{IN} - V_{TH}, & V_{IN} \leq V_{DD} + V_{TH} \quad (7.1) \\ V_{DD}, & V_{IN} > V_{DD} + V_{TH} \quad (7.2) \end{cases}$$

Step 4: The fourth step for the topology selection is to implement a rail-to-rail driving concept allowing to provide an enhanced voltage level for the operation of the push-pull buffers. Little design effort is required when externally providing additional supply voltages, e.g., [51]. However, for the overall system and PCB design, this might not be practical. Especially maintaining low gate loop inductance can be challenging (see Section III). An alternative option is to generate an enhanced supply on-chip, for which different approaches have been presented. A charge pump can be used to generate the enhanced supply directly from the main supply [63] ideally utilizing the driver input signal as a clock. For this implementation, it is beneficial if the technology provides high-density on-chip capacitors and low-drop diodes to ensure a low inherent drop for the charge pumped voltage $V_{DD+} = 2 \cdot V_{DD}$-V_{T0}. Alternatively, the enhanced supply and the main supply can be generated from a single higher voltage supply V_{CC} (see also Fig. 6) with an on-chip linear voltage regulator, e.g., [53]. This avoids the necessity of low-drop diodes and possibly large on-chip capacitors for a charge pump solution. The requirements for the enhanced supply rails are determined by the device threshold and the number of cascaded push-pull buffers. Using the same enhanced supply voltage for stages with different numbers of buffers can introduce limitations according to maximum V_{GS} ratings.

To avoid this limitation, a local bootstrapping (BS) of the supply voltage can be applied as depicted in Fig. 9 for which different solutions are presented in [59]. This way a safe and full on-state of transistor M_{PU} in the push-pull buffer is ensured. Again, the availability of high-density on-chip capacitors and low-drop diodes is beneficial. The bootstrap capacitor can thereby be referenced either to the output signal of a previous stage [67], the output node of the push-pull inverter [59], or even in an interleaved way utilizing multiple BS stages that result in a charge pump [60], [64]. It is also possible to apply this approach to subsequent push-pull buffers [68]. However, including bootstrap capacitors in the drive string can slow down the circuit performance compared to a directly applied supply voltage. Furthermore, the gate structure related leakage can limit the max. on-time of the internal bootstrapped stages.

A design aspect to consider for all topology decision steps (1–4) is the input capacitance as different requirements can be introduced by control ASICs and microcontrollers or even on-chip logic due to the driving strength of their output stage. A multi-stage approach allows to scale the input capacitance, also a split-path topology can reduce the input capacitance, as the devices M_{PU}, M_{PD} controlling the power HEMT in the final stage are not directly connected to the input signal. After step-by-step topology selection, the devices must be dimensioned (gate widths, resistors, etc.) depending on the design goals.

Furthermore, additional elements can be included in the driver topology. As a solution to the voltage limitation of the push-pull buffer, a compromise is presented in [13]. Two parallel pull-up devices are implemented of which only one is controlled with an enhanced voltage input signal. This allows for a fast turn-on of the power HEMT with one device while ensuring a full-rail turn-on with the other, thereby reducing the load to the enhanced supply rail. Furthermore, a temperature and V_{TH} compensated Miller plateau sensing and corresponding drive current control is presented in [53]. For cross-conduction control, additional logic circuitry is implemented in the driver presented e.g., in [51]. Generally, additional logic circuits come at the cost of increasing the driver's propagation delay and static power consumption due to the DCFL or RTL implementation. A first comparison of

TABLE 3 Topology Selection

Path \ Stages	Single-Stage	Multi-Stage
Single-Path	++ complexity ++ area ++ propagation delay – input capacitance – design flexibility – static power	+ input capacitance – propagation delay
Split-Path	++ cross-conduction control ++ strong driving + input capacitance + static power	++ input capacitance ++ static power ++ cross-conduction control ++ strong driving + design flexibility –– propagation delay – complexity

TABLE 4 Input Data for an Exemplary Design Process

Type	Values/Comment
Application	$V_{DS} = 48$ V, $I_D = 25$ A, dV_{DS}/dt = 60 V/ns, f_{SW} = 1 MHz
Power HEMT design	EPC2218 (see. Table I)
GaN technology	p-GaN power IC technology [19,69], similar technology to that of the power HEMT
Constraints	only one supply voltage of 5 V, full rail driving
Design goals	low power consumption, fast switching

single-input unipolar GaN gate driver with rail-to-rail output has already been performed by the author in [69].

C. PRACTICAL DESIGN EXAMPLE PROCESS

In this section, the design flow (see Fig. 7) for a gate driver is run through using a practical example with a real application scenario. The input data is given in Table 4.

The design flow starts with the gate loop requirements and the calculation of R_{PU} and R_{PD}. With the values from Tables 1 and 4 (power transistor EPC2218), the following resistances can be calculated according to formula (1), (2), (3): $R_{PU,OPT} = 2.50\ \Omega$, $R_{PU,MIN} = 1.92\ \Omega$, and $R_{PD,MAX} = 4.64\ \Omega$. According to the recommendations (Section III-D and Table 2), $R_{PD} = R_{PU}$ and in this example, 2.1 Ω is chosen to cover both hard- and soft switching in the application. The push-pull stage is implemented with two e-mode HEMTs. In order to have a certain safety margin to the supply voltage V_{DD} of 5 V, devices of the 12 V-class are selected. These e-mode devices have an on-resistance scaled to the gate width of 6.3 Ω×mm [64], [69], which results in 3 mm gate width to realize a 2.1 Ω on-resistance.

Next comes the gate driver topology selection using the step-by-step guide (see Fig. 9). Step 1: A single path topology is selected due to its lower complexity and shorter propagation delay time. Step 2: A multi-stage approach is chosen to ensure a low input capacitance while ensuring strong drive strength in the last stage. Step 3: The stage building of the topology consists of two stages, as these allow a good trade-off between power consumption and switching time. The input stage is a simple inverter and the output stage is a push-pull stage, where the signal for the pull-up device is provided from another simple inverter. The topology is shown in Fig. 8. Due to the technological possibilities, the simple inverters are designed as DCFL inverters for optimal power consumption and chip area [69]. To specify power consumption requirements using (4), the gate charge losses can be calculated, which in this case sum up to ∼30 mW. Reducing the switching frequency by a factor of 10 would result in the same reduction of gate charge losses. For the non-switching case, the quiescent current is targeted not to exceed 2 mA (at 5 V, 10 mW), while the power consumption at 1 MHz should be <40 mW. Step 4: The boundary conditions are decisive for the rail-to-rail driving concept. Only one supply voltage of 5 V is available (see Table 4), which means that only a charge pump or bootstrapping can be considered. For the bootstrapping of the last stage, an on-chip capacitance in a range >30pF is needed. This value can be reduced by the charge pump supply approach. The detailed schematic is shown in Fig. 10 [60], [64]. The charge pump consists of two e-mode HEMTs with on-chip capacitors.

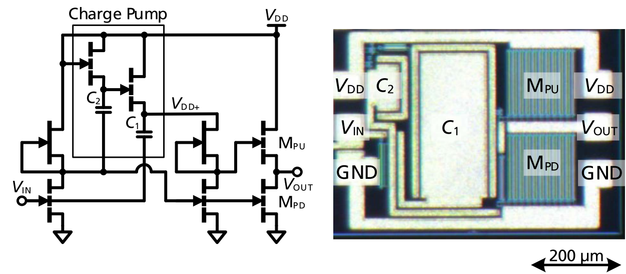

FIGURE 10. Schematic and chip micrography of the gate driver design.

The next step is to design the circuit of Fig. 10. The circuit is simulated with Advanced Design Software (ADS) PDK of the p-GaN power IC technology [19], [69] of the Fraunhofer IAF and optimized for low power consumption (<40 mW at 1 MHz) and high switching speed. After that, the GaN driver is fabricated using the same technology. Fig. 10 shows a chip micrograph of the IC. The total chip area is 0.291 mm^2 (see Fig. 10, 640 × 455 μm^2). All transistors of the driver are 12 V-devices. The gate width of the pull-up MPU and -down MPD device is 3 mm each. Both DCFL inverters have gate widths of 10/100 μm for pull-up and -down device. The input capacitance of the input transistor has less than 1 pF and the threshold voltage is <2 V, allowing the driver to be directly controlled by MCU, DSP, ASIC, or input logic implemented in GaN (see Fig. 6). The 2DEG-stacked MIM capacitors $C1$ and $C2$ have a capacitance of about 50 pF and 5 pF showing a capacitance density of 1.2 fF/μm^2 (see Section II). Compared to conventional MIM capacitors (typ. 0.3 fF/μm^2 [25]) this saves 3/4th of the chip area, which is a lot considering the chip micrography. The realization of high-density on-chip capacitors is crucial for the rail-to-rail driving concept. More details about the technology can be found in [19], [69].

Fig. 11 shows simulated and measured supply power consumption as a function of the switching frequency with supply voltage of 5 V, different duty-cycles DC and three load

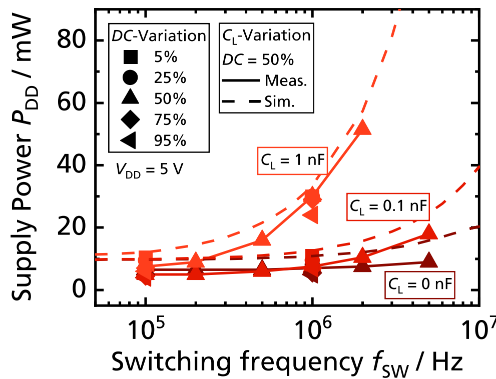

FIGURE 11. Simulated and measured power supply as function of the switching frequency with five different duty-cycles (*DC*) and three load capacitances.

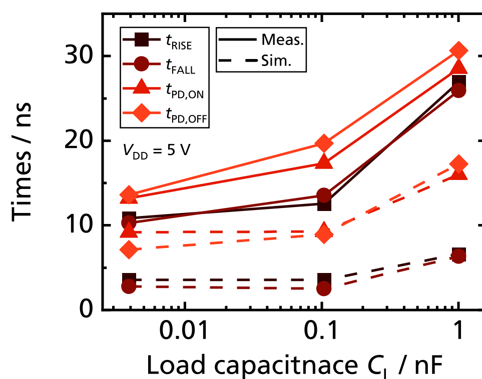

FIGURE 12. Simulated and measured rise t_{RISE}, fall t_{FALL}, turn-on $t_{PD,ON}$, and turn-off propagation delay times $t_{PD,OFF}$ for three load capacitances.

capacitances. The load capacitance of 1 nF corresponds approximately to the input capacitance C_{ISS} of the power HEMT EPC2911 (see Table 1). If the *DC* increases, the current decreases, because the time of the output low state of the inverter T_{LOW} decreases (see Section IV-B). The simulation and the measurement show identical progressions. The design goal of a power consumption <40 mW at 1 MHz is thus achieved (simulated 33.5 mW and measured 30 mW with 1 nF). The maximum switching frequency is >5 MHz. Fig. 12 shows a simulation and measurement of the rise t_{RISE}, fall t_{FALL}, turn-on $t_{PD,ON}$, and turn-off propagation delay times $t_{PD,OFF}$ for three load capacitances with V_{DD} = 5 V (the passive probe capacitance of 3.9 pF is also included). The measured times are larger than in the simulations, most likely due to the additional parasitic capacitances due to the IC test packaging (in this case a DIL package). Thus, an optimized GaN gate driver in terms of losses and switching speed is achieved as a result or outcome of the design flow.

V. CONCLUSION

Due to various benefits in terms of speed and parasitic effects, the first step in monolithic GaN integration is the functional integration of the gate driver together with the power HEMT. This work describes the GaN gate driver design in a design flow. First, an insight into GaN technologies and their possibilities in terms of IC design is given. The driving of GaN power HEMTs is described with the requirements for the gate loop and its dimensioning. As background, topology research was performed and a step-by-step guide is introduced for the selection of the topology. This guide contains 4 steps: single or split path, mono or multi-stage, stage building, and rail-to-rail driving. Finally, the design flow is run through with an application scenario as an example. A GaN gate driver optimized for losses and speed is the result verified by simulation and measurement. Thus, this work provides a design guide for monolithically integrated GaN gate drivers.

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