Designing, simulating and modelling EMC-Filters for a GaN-based Bi-directional On-Board Charger

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1 Introduction

The latest forecasts for the electric car industry worldwide indicate an important rise of e-mobility. Subsequently the high demand of on-board charger (OBC) has gained a major significance in any electric vehicle. In order to reduce weight and size – affecting efficiency and costs – wide band-gap devices such as gallium nitride (GaN) are a good choice for power conversion. They are well known for a low output capacitance (C_{OSS}) that enables them to switch faster and more efficiently than traditional silicon metaloxide semiconductor field-effect transistors (MOSFETs), enabling a considerable reduction in the volume of the OBC but tend on the other hand to increase substantially the electromagnetic emission.

This article reviews EMC filter design, simulation and modelling best practices for reliable data enabling designers to optimize before hardware is available. Iterating between modeling and simulation for the EMC-Filter can improve the quality of the system design early, reducing the number of errors found later in the design process. Well known modeling methods and simulations can give a first approximation of the disturbances and their behaviour changing the circuit parameters. Later we discuss the impact of GaN and isolation transformer on the electromagnetic interference (EMI) spectrum, and possible ideas to help troubleshoot conducted emissions problems observed from simulation results.

2 Simulation for Prediction of conducted emissions

Figure 1 shows the architecture of the selected smart GaN bi-directional OBC based on 650 V GaN Enhancement mode High Electron Mobility Transistor (E-HEMT), with a particular focus on the GS66504B bottom-side cooled transistor as our chosen sample for the first prototype. The converter in question is rated at 6 kW, with a targeted power density of 2 kW/l. In addition to the architecture, there is a list of specifications that have been defined. It includes the information/data of building blocks, the expected interfaces, power converters (AC/DC and DC/DC), protection devices, AC input, DC output, and measurement units. Based on this three-phase prototype, a simplified single-phase version is designed for simulation results and evaluated to demonstrate which characteristics can be identified in an early design phase of the converter and EMC-filter development. The bi-directional bridgeless power factor correction (PFC) for AC/DC power conversion and the dual active bridge (DAB) circuits are modelled and simulated using LTspice environment. LTspice contains many units used in switch-mode power supplies and can run lots of models created by MOSFET manufacturers. Therefore, it has a wide user network [1]. Considering the switching frequencies of both converters, the simulated conducted emission is discussed.

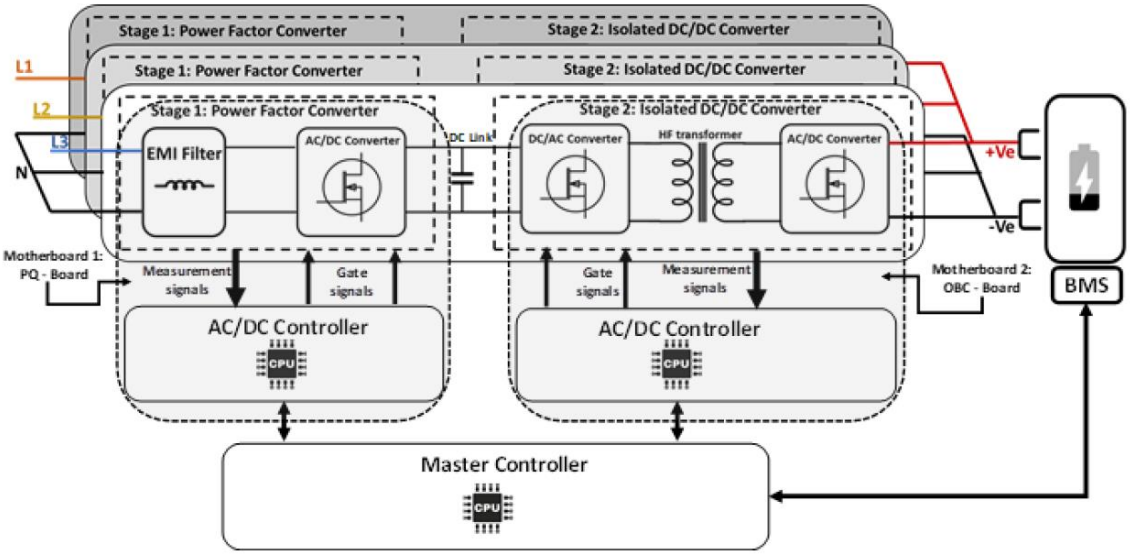

Figure 1: Interconnection block diagram of the on-board charger

To fulfill the known tasks of an Artificial Mains Network (AMN) a model of single phase of it shall comply with the requirements of CISPR 16-1-2 with 50 Ω || 50 µH.

2.1 Simulation approach of common- and differential-mode separator

Measurement receivers and spectrum analyzers in a standard AMN setup measure an unsymmetric voltage. The phase information is lost in the process. To measure the common mode (CM) and differential mode (DM) disturbance voltages, the nodal interference voltages must be added or subtracted in phase, which is done before getting to the measurement receiver with an additional analog circuit. Additionally this circuit has many measurement modes to expand the measurement possibilities of two V-Line Impedance Stabilisation Network (LISN) to T- and Delta-LISNs for the profound analysis of interference emissions. They mostly consist of Radio Frequency (RF) transformers which add or subtract the applied voltages according to their winding sense.
The performance of a CM/DM separator is characterized by four parameters:

1. CM transmission ratio (CMTR)
2. DM transmission ratio (DMTR)
3. DM rejection ratio (DMRR)
4. CM rejection ratio (CMRR).

For CMTR and DMTR, the insertion loss should remain below 2 dB, which is defined as measurement uncertainty in CISPR 16-1-1 for sinusoidal signals [2] sec 4.3. In CISPR 16-1-1, it is stated that the difference between signal and background noise should be an attenuation of at least 20 dB. In research studies, there are two passive separator topologies that satisfy the requirements, proposed by Nagel [3] and Wang [4]. The proposed simple CM/DM separator Model is shown in Figure 2. Two input ports and two ports for CM- and DM-output. The selected 1:1 transformer here is a common mode choke with 500 µH inductance and leakage inductance of 75 nH. The proposed CM/DM Separator was investigated and verified. Conducted emission on HV+ and HV- of the DC-output of DC-DC converter were simulated in frequency domain taken into account the paramaters that are important for an accurate FFT analysis. This may be plotted directly on LTspice considering the relationship between the default LTspice unit as dBV and dBµV used typically in conducted emission measurements in a lab.

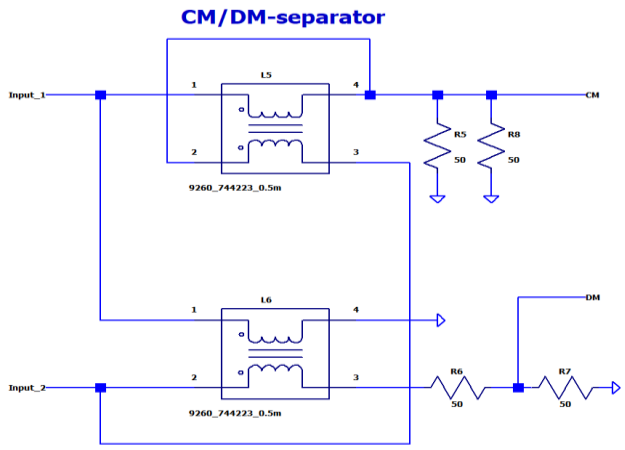

Figure 2: Proposed CM/DM noise separator

To increase the simulation accuracy for frequencies above 30 MHz, both the interference source and the transmission path to the AMN must be modeled in detail. A well known approach [5] is based on a combination of transient circuit simulation with a 3D simulation in the frequency domain.

2.2 Bi-directional bridgeless PFC Model (AC/DC)

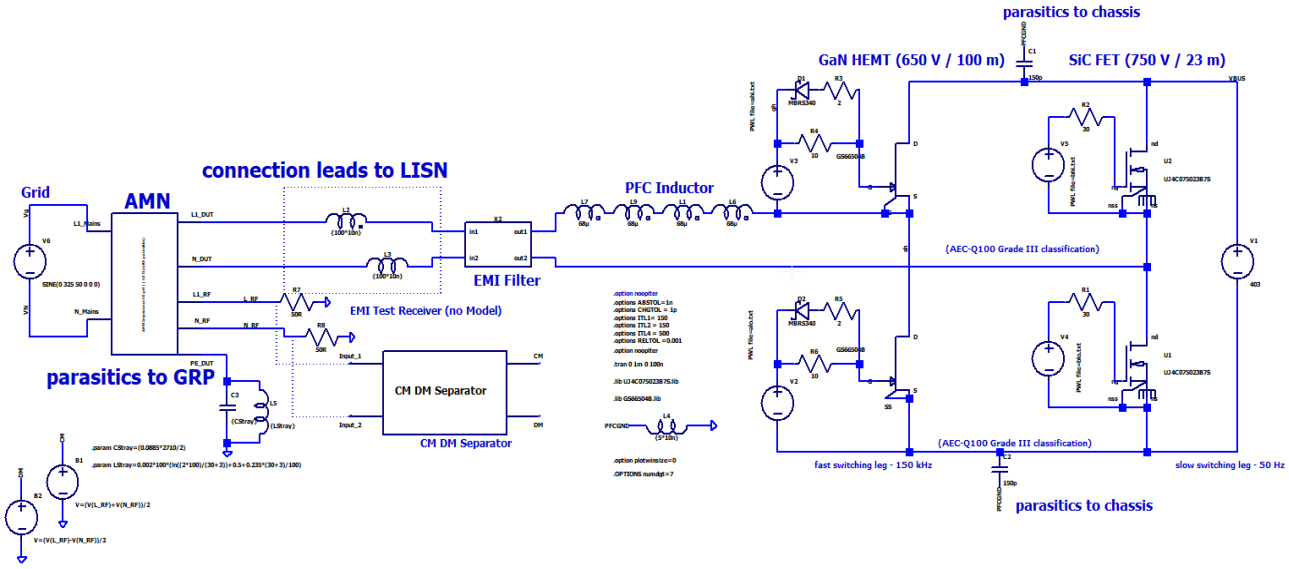

Figure 3: Bridgeless Totem Pole-PFC (BTP-PFC) Circuit with EMC filter

The development trend of on-board chargers is moving towards bi-directional operation, it enables power flow control from the grid to the vehicle (G2V) and back to the grid (V2G). The non-interleaved AC/DC stage is based on a BTP-PFC topology. For simplicity a single-phase BTP-PFC is shown in Figure 3 instead of three-phase BTP-PFC. To meet the EMC requirements, an EMC filter is added between the topology and AC source to attenuate the noise coming from the high-speed switching behaviors of the BTP-PFC. Such systems are designed for high efficiency due to neglected bridge diode loss compared to a conventional Boost PFC. The selected transistor models on the fast-switching leg (FS-leg) present the wide band-gap devices (e.g. GaN HEMT) while the slow-switching leg (SS-leg) commutates at the grid frequency (e. g. 50 Hz) with Si or SiC switches. The absence of reverse-recovery behavior for the GaN HEMT is expected to result in reduced EMI generation caused by high switching di/dt [6]. The generated noise has dv/dt and di/dt switching behavior with ripple current on the the PFC inductor.

In theory, for a given power rating and ripple current of PFC inductor, the 1st peak noise amplitude $U_{L\_RF_{pk}}$ can be estimated by the equation [7] below:

$$U_{L\_RF_{pk}} = 20 \cdot \log\left(FFT(i(t)) \cdot \mathrm{Z_{in}} \cdot 10^{6}\right) \qquad 1$$

Where the input inductor current i(t) is the sum of the ripple current Δi(t) and the AC line frequency shaped current, the ripple current of PFC inductor is influenced by these parameters: the inductance, switching period, duty cycle, and input/output voltage; Z_{in} is the input impedance.

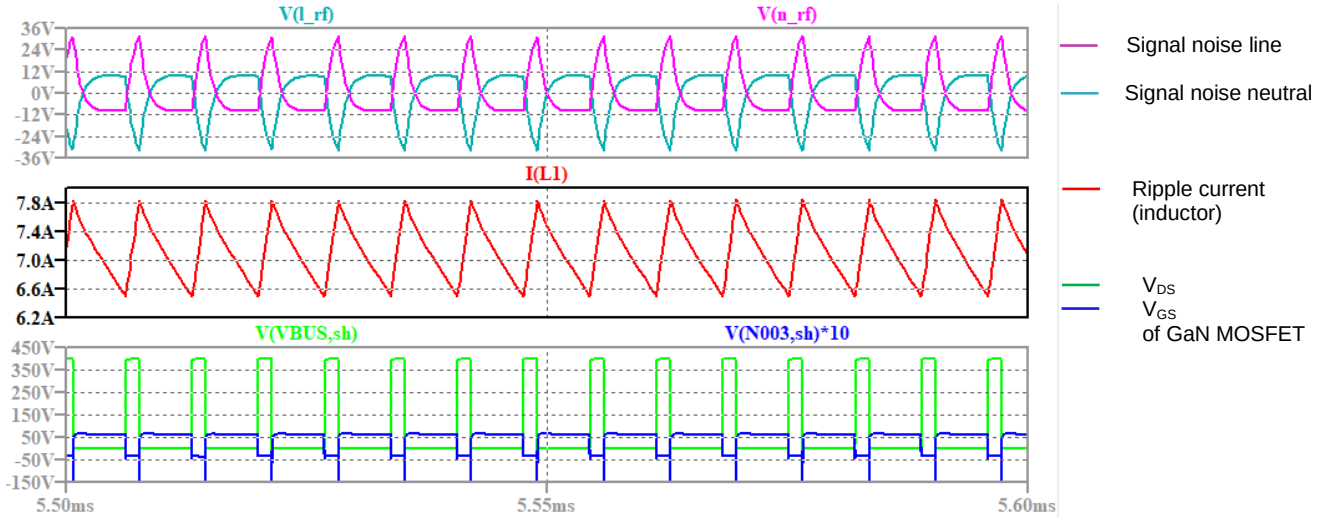

Figure 4: Signals in time domain

Figure 4 shows a section from the inductor ripple current. The steady state is reached after 5 milliseconds. To reduce ripple current, an EMC filter is mandatory. The inductor current ripple is designed to be less than 20 % of peak input current. The switching frequency (145 kHz) can be seen in the frequency domain.

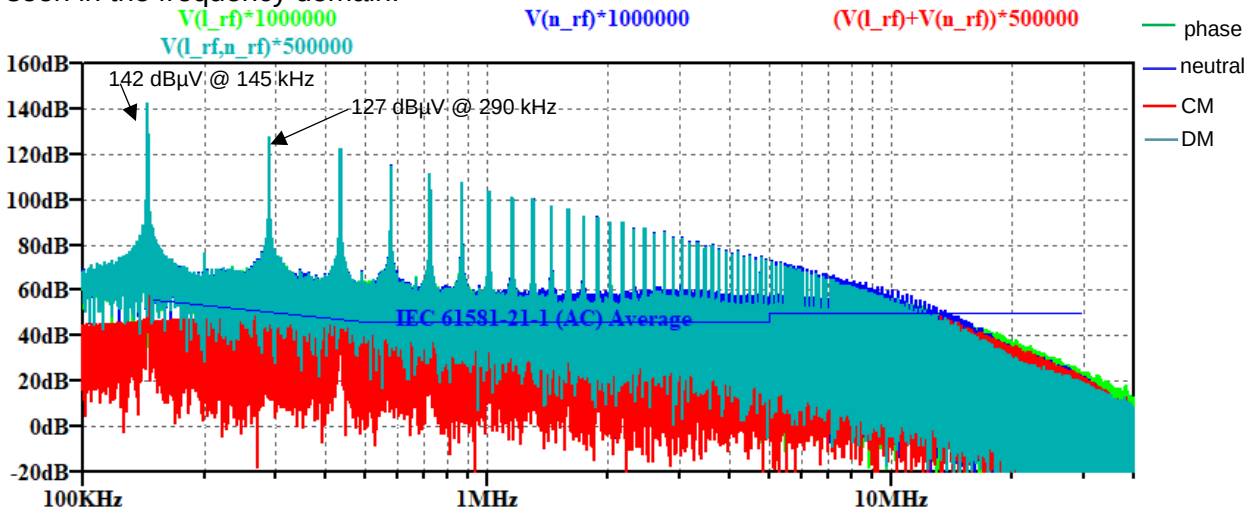

Figure 5: Simulation of conducted emission AC port without EMC filter; phase (green), neutral (blue) common mode (red) and differential mode (cyan)

From the results above (Figure 5) on AC port without EMC filter, a quite high filter attenuation of around 80 dB is needed to meet the limit (at about 300 kHz). The resulting switching frequency of 145 kHz is helpful to keep the filtering expense low, because the fundamental frequency stays below the frequency range (150 kHz … 30 MHz) of conducted emission limits defined. Depending on the character of signal noise, different filter components are efficient. However due to one of the main objectives of the project – a compact design – a two-stage filter design is out of question. That may result in some compromise when realizing the filter.

As suggested, the separation of common mode and differential mode signal noise is useful, but separated CM and DM are only valid if the system is strictly symmetrical. In practice, power electronic systems are usually unbalanced to some degree. Due to an unbalanced system, the CM disturbances are observed in the DM signal and vice versa, as mode conversion.

2.3 Dual-active Bridge Model (DC/DC)

This model is simulated for maximum power operation (single phase shift), The single-phase DAB consists of two voltage-driven full bridges, a high-frequency transformer operating with a nominal frequency of about 500 kHz and the DC link bus. The DC voltage source from the AC/DC converter provide the necessary voltage for the full bridges of the DAB on the primary side. In practical applications, the voltage is stabilized by sufficiently large capacitances on the respective sides. The power is typically transmitted to the secondary side through a transformer with a transformation ratio n galvanically separated from the primary side. Different from the AC side, the power supply on the secondary side was modelled using an artificial network (AN) defined in CISPR 25.

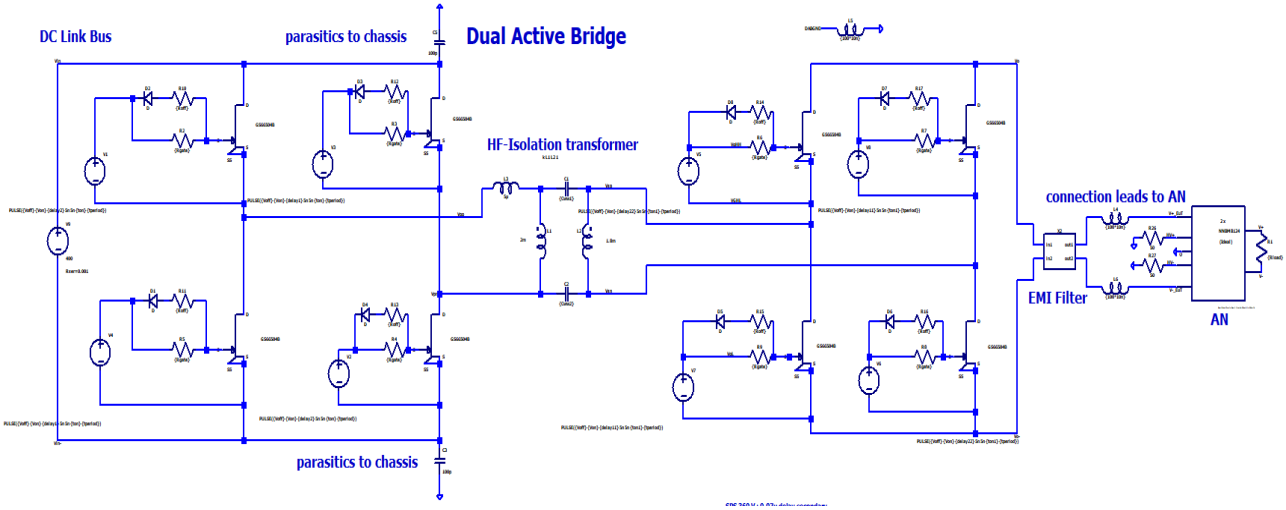

Figure 6: Dual Active Bridge (DC/DC) for single phase and setup with AN (CISPR 25)

The slightly different impedance of the AN and the higher limits in comparison to the AC side results in much less strict requirements.

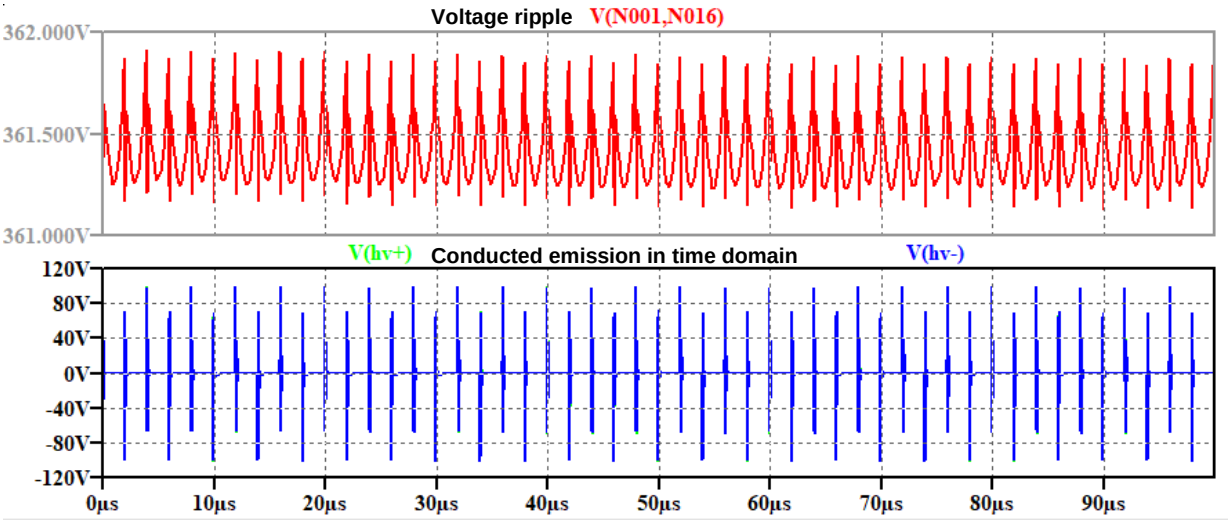

Figure 7: Voltage ripple (top) and conducted emission (bottom) in time domain – without EMC filter (only 2.2 µF smoothing capacitor)

The resulting switching frequency of 250 kHz of each full bridge is higher than on AC/DC stage. From results below, It is clear that for such filtering a common-mode choke plays a particularly important role. Improved EMI control in PCB design and to follow the guidelines to minimize EMI issues are essential during the design process.

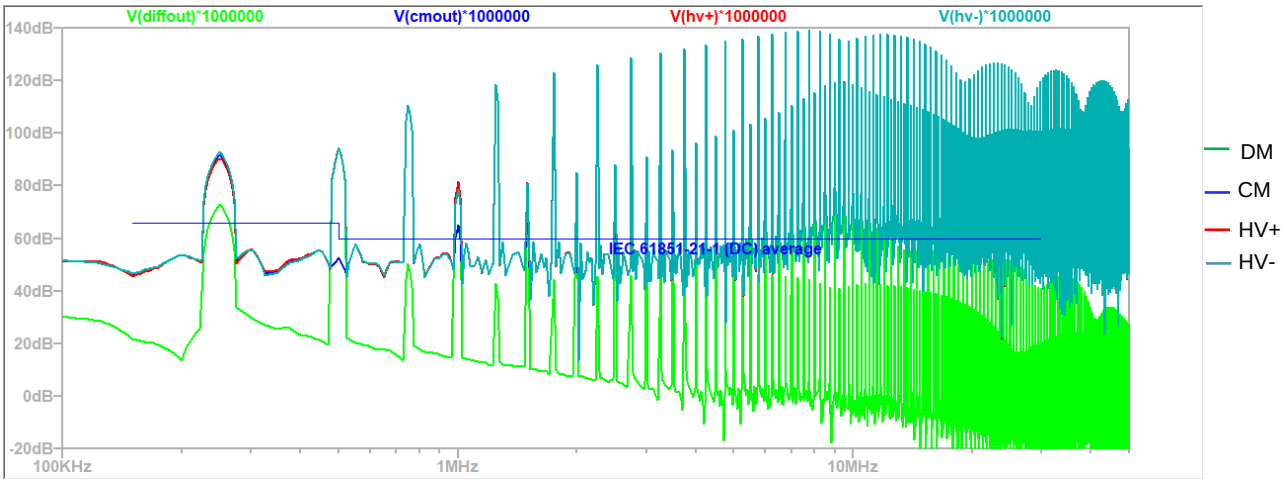

Figure 8: Simulation of noise spectrum without EMC filter; dominant common mode

3 EMC-Filter Design and Simulation Model

The OBC AC-DC 6 kW converter will be equipped with a planar copper cold plate, this cold plate is of particular importance to the EMI discussion because it connects to ground; any parasitic capacitance to the cold plate therefore has the potential to guide common-mode emissions. The volume of the filter plays a big role from size perspective. As a target it should occupy in between 35 to 39% of the input board (AC-side). Further investigations were carried out to verify the option of reducing noise level on changing the switching behaviour of the GaN MOSFET (R_{gate} turn on and off resistors) and also to get some idea about the parasitic components of the isolation-transformer of the DC/DC converter in this early design stage.

3.1 AC-side

It is possible to realize the first design of the EMC filter from the insertion loss (IL) specifications. Since the DM inductance depends on the leakage inductance of theCommon-Mode Choke (CMC), the CM filter is designed first. Since a low-pass attenuation is needed, a power line filter is based on an LC topology. In particular, the simplest topology of a filter is composed of a CMC together with two Y-capacitors for the CM emission, and by two differential-mode inductances combined with an X-capacitor for the DM component. Since IL_{CM} = 80 dB at 150 kHz is needed, considering that the filter is a 2nd order filter, its attenuation increases with a −40 dB/dec after the corner frequency, which has to be chosen between 5-10 kHz. The CM inductor is given by the resonance frequency of the LC low pass filter characteristics.

$$L_{CM} = \left(\frac{1}{2\pi f_{CM}}\right)^2 \cdot \frac{1}{2C_y} \qquad 2$$

Because a two stage filter is out of question – compact and small design – one stage should remain with a compromise to take the inductance value up to 2…3 mH. Since the DM filter needs about 80 dB attenuation as the CM Filter (symmetrical circuit assumed). IL_{DM} = 80 dB at 150 kHz, a corner frequency of f_{DM} = 10 kHz has been considered, providing

$$C_X = \frac{1}{2\pi f_{DM} 2L_{DM}} \qquad 3$$

Where L_{DM} is the leackage inductance of the common mode choke $L_{DM} = L_{CM} \cdot (1 - k^2)$. These values are needed to make a first simulation of the filter. Further optimizations and component selection based on specifications and the solution proposed by the main semiconductor and magnetics manufacturers for EMI suppression applications were taken into consideration.
The first quick steps were to simulate such a filter construction with ideal components and then implement parasitics on the simulation setup and make conclusions about chosing the right components for filtering out the noise keeping in mind that simulations are mostly significant up to a frequency of 1 MHz. it is always helpful to meet EMC requirements on simulation with a margin bigger than 6 dB for any uncertainities during simulations and design process of the circuit.

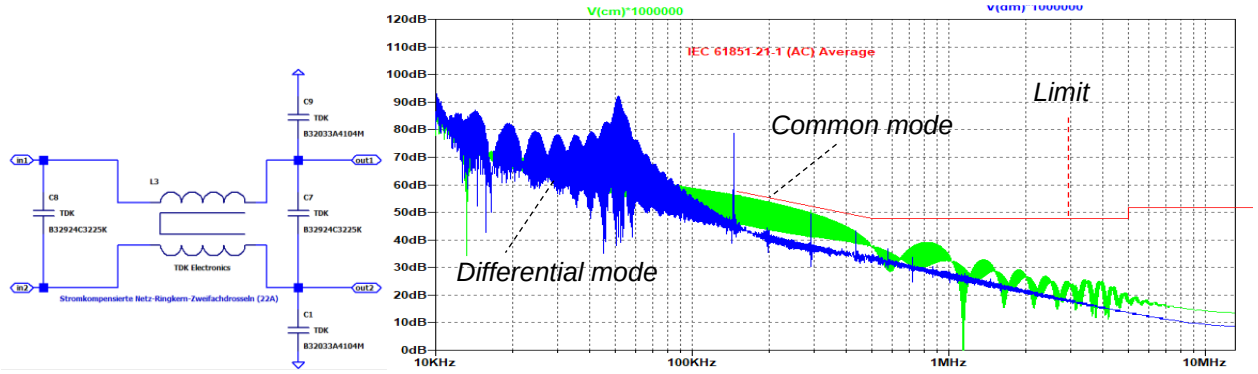

Figure 9: Simulation results with single stage filter given in the figure left.

Due to real RF components, the insertion loss of 80 dB for the EMC filter are at 300 kHz instead of 150 kHz. This is an essential step during the design process of selecting the right components that effectively achieve the desired attenuation (e.g. using algorithms to iterate through all useful and possible parameters and their combinations).

3.2 DC-side

At the HV DC output of the OBC, any remaining harmonics should be filtered out in order to meet requirements on this port. Specific components are normaly used in this stage to handle the extreme power conditions that occur in an Electric Vehicle (EV) output filter. They should not only withstand electrical characteristics, but also the physical characteristics required during operation. The same approach for filter attenuation required on the AC side was carried out for the DC Filter.

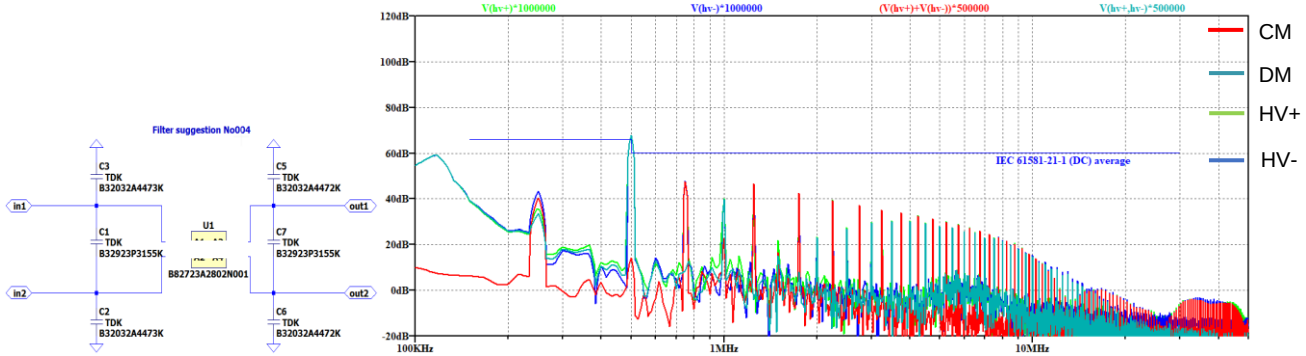

Figure 10: suggested output filter with CMC 540µH, 2x 1.5µF X-capacitors, 2x 47nF Y-capacitors, 2x 4.7nF Y-capacitors (top); noise level with filter (bottom)

The proposed common mode choke will be for automotive purpose, therefore a more accurate advanced model to reduce noise level on the frequency range of about 500 kHz is the next step to optimize filter performance before taking further actions at this design stage. Volume and part list of the proposed filter are shown in the following table:

Component	stage	Part-Number	WxHxL [mm]	quantity	Volume
C_Y – 47nF	1	B32032A4473K	9.0x17.5x18.0	2	5.7
CMC	1	customer project no.	25x33.5x33.0	1	15.9
C_X – 1.5uF	1/2	B32923P3155K	14.5x29.5x26.5	2	22.7
C_Y – 4.7nF	2	B32032A4472K	5.0 x10.5x18.0	2	1.9
Sum					46.2 cm³

Loss estimation in LTSpice: 38.7 W; DC link capacitor current: 1.92 A_{eff}
It is helpful specifically to adjust the components with further measures or make a better choice of an appropriate RF advanced filter model.

4 Conclusion

This article describes conducted emissions of the selected GaN based bidirectional on board charger varying the complexity for filter development and modeling methods for more accurate results before completion of the first prototype. The described circuit simulation in the time and frequency domain has so far made it a usefull tool to predict conducted emissions in a IEC 61851-21-1 measurement enviroment, analysing EMC filter needs and their optimization. Incorrectly assumed parameters of the GaN transistor drivers or the RF isolated transformer of DC/DC converter are identified as additional factors for the observed deviation in simulation results. To improve the accuracy, an optimization of these parameters, sampling EMC Filters and measuring their parasitics is therefore proposed. The development and refinement of suitable optimization and the associated effects during modeling process on the simulation accuracy are one of the major subjects of current work.

5 ACKNOWLEDGMENT

This work was supported by HiEFFICIENT project. This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement no. 101007281. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Austria, Germany, Slovenia, Netherlands, Belgium, Slovakia, France, Italy, and Turkey.

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