An Integrated Heated Testbench for Characterizing High Temperature ICs

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***Abstract*—This paper presents a newly developed integrated heating system, which can keep the IC under test at a constant temperature of up to 250 °C. The heating system can be used while the IC under test is mounted on its custom-designed interface board, which controls the two supply voltages and provides connectivity to an FPGA. Using a testing framework on the FPGA, the test stimuli and operating clock can be provided with at least 100 MHz. Thus, it is possible to fully vary all three parameters—frequency, voltage, and temperature—during continuous operation of the IC. A case study is performed with a previously fabricated ASIC to test the proposed system.**

I. Introduction

Some applications require integrated circuits to operate under extreme conditions, such as mechanical vibrations, unreliable power supply, and high temperatures. For example in geothermal drilling, the drill bit has to be directed along a planned path underground. Since the uplink to the surface is very limited (in the order of a few bits per second), measurement and data processing is ideally performed downhole. However, the high environment temperature and heat generated by drilling require the electronics to operate at temperatures above 200 °C (as shown in Table I).

In a previous work [1], an application specific integrated circuit (ASIC) containing different approximate adder architectures was designed, simulated, and subsequently manufactured. In order to verify the simulation results and assess the real-world performance of the fabricated chip under different operating conditions, specialized testing equipment is necessary. A special printed circuit board (PCB) was designed to host the ASIC and provide a programmatically adjustable power supply, as well as connectivity to an FPGA-based platform which can generate test stimuli at variable clock rates. This enables characterization at various supply voltages, but does not allow testing the ASIC in realistic high-temperature environments.

In order to test the ASIC at higher temperatures, a specialized heating system is needed. Simply placing the whole test setup in a climate chamber is not feasible, because all parts system—besides the ASIC—use off-the-shelf components which are only rated for operation up to roughly 85–100 °C. This work presents a newly developed integrated heating system, which can keep the ASIC at a constant temperature of up to 250 °C, while all other components are kept relatively cool. The heating system is mounted on its custom PCB, allowing the ASIC to operate normally during heating. By integrating the heating system into the FPGA-based control system, it becomes possible to vary all three parameters—frequency, voltage, and temperature—and, thus, perform a complete characterization of the ASIC.

TABLE I
Different temperature requirements for several high temperature semiconductor applications [2], [3].

Application Domain		Temperature
Automotive	Driver interior	−40 °C to 85 °C
	Underhood	−40 °C to 125 °C
	On-engine	−40 °C to 150 °C
	Exhaust & combustion areas	−40 °C to 200–600 °C
Drilling	Downhole well logging	≥ 200 °C
Aviation	Distributed Engine Controller	−55 °C to 225 °C

This paper is organized as follows: The proposed heating system architecture is introduced in Section II, where the individual constituents of the system are discussed. The results of the simulations and measurements are presented in form of a case study in Section III. A conclusion is given in Section IV.

II. Proposed Heating System

As depicted in Fig. 1, the heating system comprises four main parts: The heating chamber, which contains the device under test (DUT) mounted on the test PCB, the temperature controller, an FPGA-based test interface, and a host PC, which runs a MATLAB or a Python script to control the whole experiment schedule. The following sections describe the function and the purpose of the individual components in greater detail.

A. Heating Chamber

The heating chamber consists of a *thermal insulation box* made of foam glass, which contains the *DUT* in a high-temperature ceramic pin grid array (PGA) package (shown in Fig. 2). Long *extension pins* perforate the isolation box in order to establish electrical contact to the *testing PCB*, which provides connectivity to the FPGA-based test interface. In order to spread the heat generated by the *ceramic heating element* uniformly to the whole DUT package, both components are mounted on a *copper heat spreader*. Two *type-K thermocouples* serve as a feedback path to the proportional-integral-derivative (PID) controller, which is designed to keep the temperature on the die constant.

Since the zero insertion force (ZIF) socket used to mount the DUT to the test PCB is not suitable for operation over 140 °C, it needs to be physically separated from the heated DUT. This is achieved by extending each pin of the DUT with

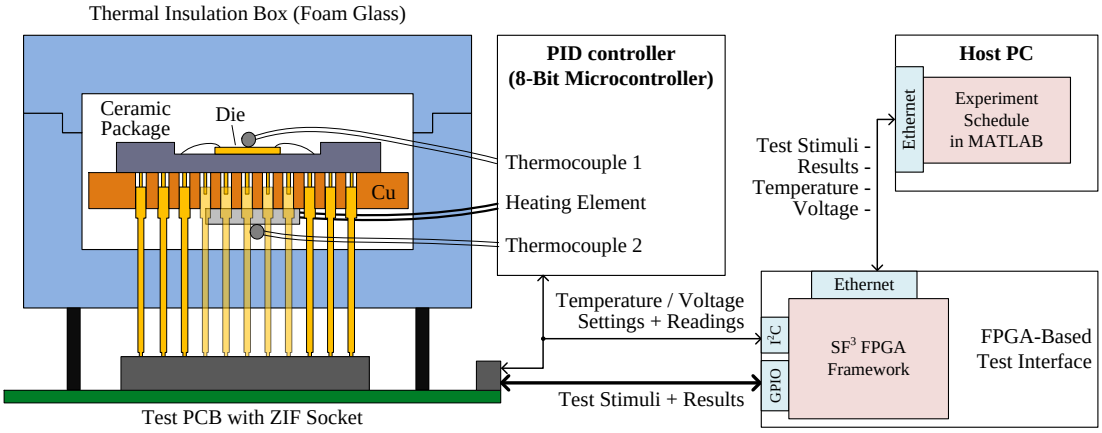


Fig. 1. General setup of the heating chamber. The DUT is mounted on a copper heat spreader and placed in a thermal insulation box, which is punctured by the connection pins. A ceramic heating element heats the DUT, while two type-K thermocouples continuously measure the DUT and heater temperatures.

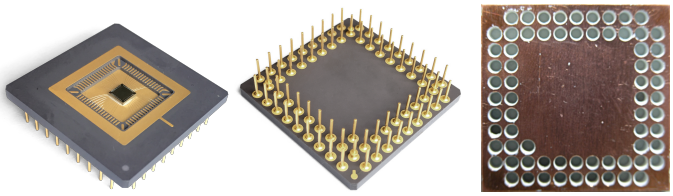
two 18 mm long extension pins and then inserting these into the ZIF socket.

The heat in the system comes from a ceramic heating element, which is basically a resistor in a flat rectangular package. The power output of the heater can be adjusted using a relatively slow pulse-width modulation (PWM) signal at around 50 Hz with adjustable duty cycle.

Attaching the heating element to the DUT requires some consideration because the metal pins used to connect the DUT to the testing PCB conduct a non-negligible amount of heat. It is thus necessary to take them into account when considering the heat distribution inside the DUT package. The metal pins have a high thermal conductivity, so simply attaching the heating element to the bottom of the package (seeFig. 2) would result in a relatively large thermal gradient inside the package because the pins would act as a heat sink (as shown in Fig. 3 b). Thus, a copper plate was designed to fit between the heating element and the DUT package, enclosing the extension pins, as depicted in Fig. 1. Since copper has a very high thermal conductivity, its temperature distribution should be relatively uniform, which also ensures that the temperature distribution inside the package is not disturbed by heat flowing through the pins.

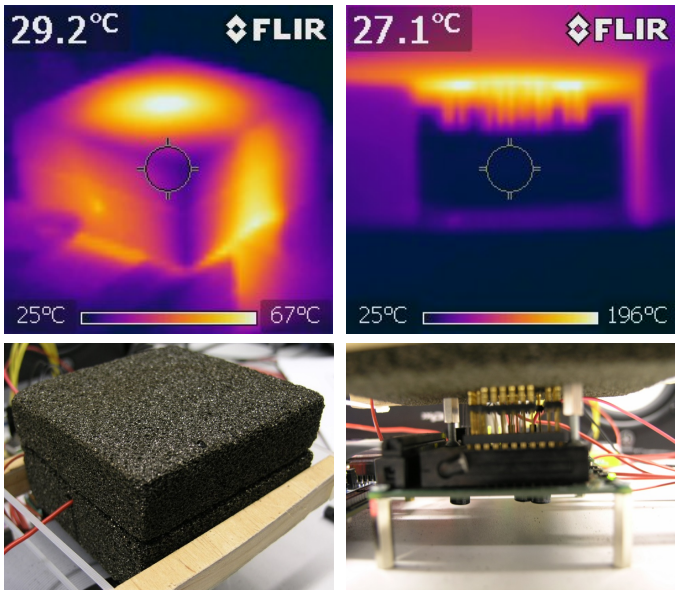
In order to prevent electrical contact between the copper plate and the gold-plated pins, the holes in the plate were coated with a thin layer of non-conductive high temperature paint. To prevent the paint from being scraped off due to motion, for example when carrying the system, the pins were the glued to the holes using a non-conductive epoxy resin.

For measuring the system temperature, two type-K thermocouple are used: One is positioned directly on the DUT and its measured temperature is used directly to control the DUT temperature. The second thermocouple is placed below the heating element and serves to ensure that the heating element does not exceed its rated temperature of 300 °C. To ensure this requirement, the temperature controller throttles the heating process when the temperature of the second thermocouple reaches 300 °C.



(a) (b) (c)

Fig. 2. (a) & (b) The ASIC which was used as a case study for the development of the heating system. (c) The copper plate used as a heat spreader to counteract the cooling effect of the pins.



(a) Insulation Box (b) Extension Pins

Fig. 3. Two perspectives of the insulation box, both as thermal images and corresponding real images, while the inside is heated to 250 °C. Images (a) shows the whole box, while (b) displays the extension pins which connect the DUT to the test PCB. Note that the test PCB is absent from the infrared image (b), which shows only the pins hanging in the air below the insulation box.

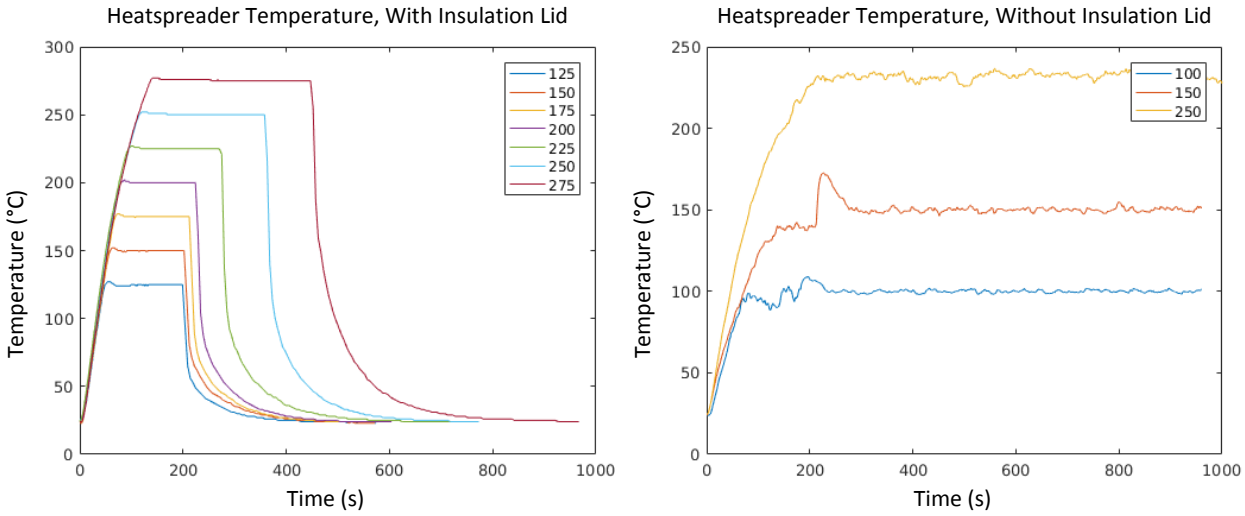


Fig. 4. Temperature traces for different temperature setpoints for system operation with and without the lid of the insulation box. In this heating test, the controller waits until the temperature is stable for a while and then cools down the system again. Without the lid, the temperature is so unstable that the controller does not initiate the cool-down cycle.

B. Insulation Box

One of the most critical parts of the heating chamber design is the enclosing insulation box. It prevents the heat from escaping through convection, which would otherwise lead to two critical problems, both of which can be seen in Fig. 4: Firstly, higher heat loss means larger temperature gradients inside the package and the die, which would ideally be at a uniform temperature to ensure stable test conditions. And secondly, the convection leads to larger fluctuations and a less stable temperature at the die.

The first effect can be seen in in the maximum temperature reached in the experiment without the lid. For the setpoint at $250\,^{\circ}\mathrm{C}$, the target temperature is not reached because the PID controller limits the temperature at the lower thermocouple near the heating element to the rated temperature of $300\,^{\circ}\mathrm{C}$. Due to the heat loss from the missing lid, the temperature gradient exceeds $60\,^{\circ}\mathrm{C}$ and the maximum temperature reached is $240\,^{\circ}\mathrm{C}$ instead of the target $250\,^{\circ}\mathrm{C}$.

The second effect is visible in the very noisy temperature measurements without the lid. Every air current near the DUT automatically reduces the temperature by a few degrees, which the PID controller immediately aims to counter by increasing the power output of the heater. Due to the relatively slow heat transfer between heating element and the die thermocouple, this correction does not immediately affect the DUT, thus leading to the observed fluctuations. Since the experiment controller waits for the temperature to remain stable within $\pm 0.5\,^{\circ}\mathrm{C}$, it does not initiate the cool-down phase of the experiment schedule in this setup.

C. Temperature Controller

In order to ensure that the DUT temperature conforms to the desired setpoint and remains stable, a controller is needed. For reliable and stable temperature regulation, PID controllers are commonly used [4]. In this system, the controller was implemented in C on an 8-bit microcontroller unit (MCU), which is fast enough to regulate the relatively slow process with a heat conduction time constant which ranges in the order of about one second.

Instead of relying on the integrated 10-bit analog-to-digital converter (ADC) in the MCU, two dedicated MAX31855 digitizer ICs for type-K thermocouples were used. These provide an ADC resolution of 14 bits and a suitable integrated preamplifier for measuring thermocouple voltages. Additionally, they perform the necessary cold junction compensation to obtain an absolute temperature value instead of a reading that is relative to room temperature. A different setup with discrete instrumentation amplifiers was also tested in the beginning, but it was later determined that an integrated solution offers less room for mistakes.

D. FPGA Framework

All operating parameters are controlled by a Cyclone IV FPGA on a DE2-115 board [5]. The FPGA is connected to the testing PCB using a 40-pin ribbon cable, which carries an I2C bus [4] and the parallel inputs and outputs of the DUT. The I2C bus is used to set and read the supply voltage and temperature, while the parallel I/Os transmit test stimuli and results between the FPGA and the DUT at an FPGA-generated clock rate of up to $100\,\mathrm{MHz}$. The stimuli are generated on a PC using MATLAB or Python and are then transmitted to the FPGA over a network connection, using the FPGA development framework SF^3 [6], which was developed at the Institute of Microelectronic Systems (IMS) at the Leibniz Universität Hannover. The outputs of the DUT are also buffered on the FPGA and can then be retrieved by the PC using the same network interface.

The two main tasks of the FPGA in this setup are to ensure that the test stimuli are delivered to the input pins of the DUT with the correct timing, and that the output of the DUT is captured at the correct time. Because the signal propagation

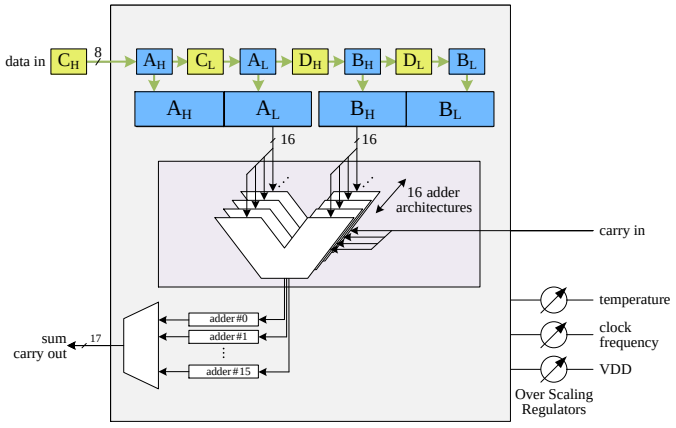


Fig. 5. Block diagram of the Stochastic ASIC [1], showing the internal structure of the data path, which contains the 16 different architectures. Since gate delay depends on the previous state of each gate in the critical path, two additions $A + B$ and $C + D$ are needed. The first addition enforces a known state, after which the result of the second one can be evaluated.

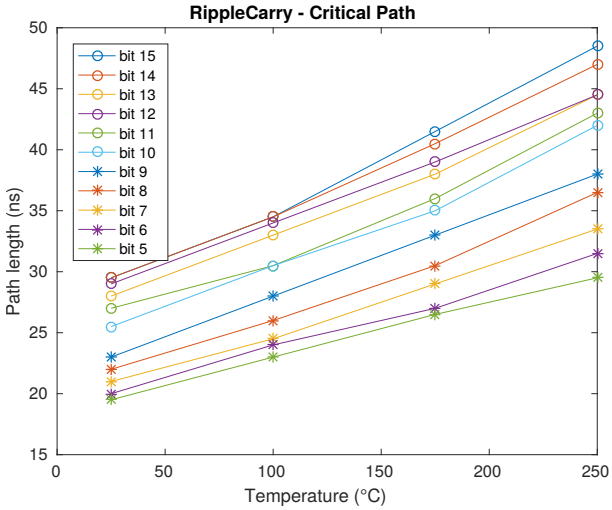


Fig. 6. Length of non-irregular RCA paths over temperature.

time from the FPGA to the DUT and back is non-negligible, extra care must be taken to ensure that the setup- and hold-times of the input registers in both devices are not violated. This requires careful tuning of the phase between the two clocks used for the DUT inputs and outputs, by calibrating the phase-locked loops (PLLs) to the specific IC that is being tested.

Additionally, the FPGA framework provides a system management bus (SMBus) master, which can also be controlled from the MATLAB or Python script over the network connection. This enables the use of an SMBus-compatible power management IC to set and read the supply voltage rails of the DUT. The MCU which contains the temperature controller is also attached to this bus, allowing the script to set and read the DUT temperature at any time.

III. Case Study: Stochastic ASIC

In this section, the heating system is evaluated in a case study using the previously implemented, simulated, and fabricated "Stochastic ASIC" [1] as the DUT. Since the ASIC was fabricated in a 250 °C high temperature SOI process, its behavior at these temperatures is especially important. The main goal of this case study is to perform an exemplified characterization of the ASIC and determine the lengths of various logic paths of the different adders contained therein.

As shown in Fig. 5, the Stochastic ASIC contains 16 different 16-bit adder architectures, including several approximate adders [7], as well as a few precise adders, such as an RCA and a carry lookahead adder (CLA), of which the last two will be examined in this case study. The inputs of all adders are coupled to the same shift registers, which enable the user to provide the four operands A, B, C, D of two consecutive additions in eight blocks of 8 bits each. As shown in Fig. 5, the eight parts of the different operands are interleaved such that the two additions $A + B$ and $C + D$ occur in two successive clock cycles. This behavior is important because the timing of an addition depends on the previous state of the adder, especially the state of the carry chain. By selecting appropriate values for the four operands, it is possible to test both transitions for each gate using the following sequence:

1) Input B_L, D_L, B_H, D_H, A_L and C_L in, as in Fig. 5.
2) Input A_H to start the addition $A+B$ to enforces a known state in the gates of the adder.
3) At the next rising clock edge, shift in C_H to start the addition of $C + D$.
4) At the next rising clock edge, capture the result of $C+D$ in a register inside the ASIC.

Based on the known state before the addition $C + D$ and the state of the individual output bits in the register, it is now possible to determine which bits were captured correctly and which were not captured because their propagation time was longer than the time between the last two rising clock edges. By trying the same additions of carefully selecting the operands at increasing clock frequencies, it is thus possible to determine the logic path lengths inside the ASIC. For an example, consider the following additions performed on a ripple carry adder:

$$\begin{aligned} A &= 1111\,1111\,1111\,1111_2 \\ B &= 0000\,0000\,0000\,0000_2 \\ \hline A + B &= 1111\,1111\,1111\,1111_2 \end{aligned} \tag{1}$$

and

$$\begin{aligned} C &= 1111\,1111\,1111\,1111_2 \\ D &= 0000\,0000\,0000\,0001_2 \\ \hline C + D_{30\,\mathrm{ns}} &= 1111\,1110\,0000\,0000_2 \end{aligned} \tag{2}$$

$$C + D_{50\,\mathrm{ns}} = \underbrace{0000\,0000\,0000\,0000_2}_{\text{Carry Propagation}} \tag{3}$$

Here, the result $C+D$ is incorrect when sampled 30 ns after the beginning of the calculation as in Eq. 2, as the most significant

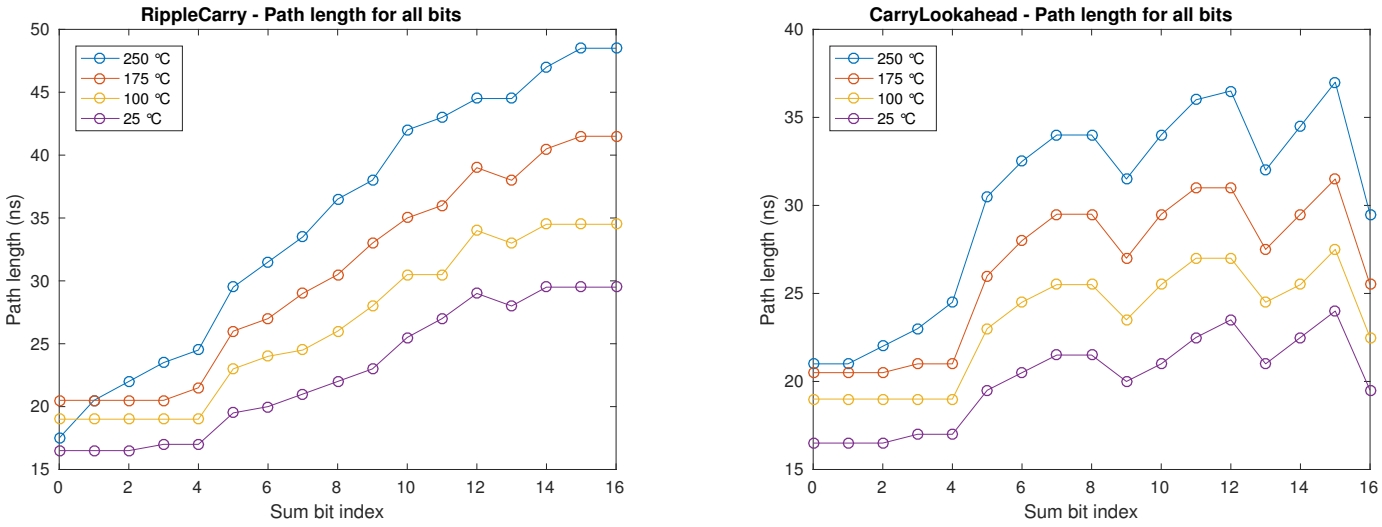


Fig. 7. The length of the critical path for each output bit of the RCA (left) and CLA (right) for different temperatures.

bits have not toggled yet. However, if the same operation is performed again and the result is sampled after $50\,\mathrm{ns}$, as shown in Eq. 3, the result is correct. This leads to the conclusion that the propagation delay of the carry chain from input bit C_0 to result bits $(C+D)_{15..9}$ must be longer than $30\,\mathrm{ns}$ but not longer than $50\,\mathrm{ns}$. On the other hand, the critical paths from input bit C_0 to result bits $(C+D)_{8..0}$ can not be longer than $30\,\mathrm{ns}$. Thus, the clock period of the highest frequency at which a given bit does not show any errors corresponds to the path length of the longest path which leads to this bit and which was affected by these operands. Of course these measurements include the propagation delay of the input shift registers, as well as the setup time of the output capture register which stores the output of the adder.

However, the carry propagation path is not always the critical path in other adder architectures like the CLA. In theses cases, a simple operand scheme like the one shown above is not sufficient to find the longest (critical) path for each individual output bit. Thus, a Monte Carlo method with a sample size of 16384 was used to find the critical paths in the RCA and the CLA with an acceptable likelihood.

The results for both adders are shown in Fig. 7, where the path length for each output bit of both studied adder architectures is plotted over the result bit index for different die temperatures. As explained above, the given path length is the lowest clock period—and thus the fastest clock rate—at which the given output bit did not show any error for all of the executed operations.

In the RCA plot, the roughly linear dependency of the path length on the bit number is clearly visible, barring some edge cases for the unlikely very long paths with a carry propagation chain of length 15 or 16, as in the example Eq. 2. Notably however, the results bits $0-3$ show a saturation behavior, where the measured path length does not depend on the bit number. This effect might be due to limitations of the measurement system and is subject to further investigation. The plot for the CLA reveals the internal block structure of the carry generator, which computes the internal "generate" and "propagate" signals in blocks of 4 bits.

Additionally, when plotting the same data over a temperature axis as in Fig. 6, it can be seen that the path length has a roughly linear dependency on the die temperature.

IV. Conclusion

The presented integrated heating system allows flexible testing of high-temperature ICs by varying factors like supply voltage, operating frequency, and die temperature. This setup enables the precise characterization of high temperature ICs for many different environmental conditions. The scriptable experiment setup allows running the characterization unattended after the initial calibration procedure. A case study has been performed to show that reliable temperature regulation and timing measurements can be achieved using the presented system.

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