

Letters

Quasi Two-Level PWM Operation of an MMC Phase Leg With Reduced Module Capacitance

Axel Mertens and Jakub Kucka

Abstract—The modular multilevel converter offers benefits for medium and high voltage power conversion due to indirect series connection of devices. The drawback is a large amount of capacitance that has to be installed in each module, often prohibiting its use in cost sensitive applications. This letter proposes a new operation mode of modular multilevel topologies that allows reducing the capacitance by at least an order of magnitude. To achieve this, the multilevel operation is sacrificed, but many advantages of indirect series connection, such as proper voltage sharing, small voltage steps, limited voltage slopes, modularity, and scalability remain.

Index Terms—Direct current (DC)/Alternating current (AC) converters, electric drive, modular multilevel converter, medium voltage, pulse width modulation (PWM).

I. INTRODUCTION

THE greatest drawback of modular multilevel topologies, i.e., modular multilevel converter (MMC) and modular multilevel matrix converter, is the energy variation at the module capacitors, which determines the required module capacitance. The module capacitors are the dominant factor for volume and cost of these converters. Several approaches were presented in order to reduce the energy variation at low output frequencies [1]–[3]. These methods do not affect the phase-to-phase output voltage. However, they do not reduce the size of capacitors to a level where they are not dominant any more.

Using an additional higher frequency for power transfer between the converter arms, also a generic dc/dc conversion was proposed [4]. Here, the output voltage also includes the additional frequency used for energy balancing, which has to be suppressed by passive filters.

Another approach is presented in [5]. Here the idea is to use the voltage variations introduced by multilevel PWM together with a circulating current to compensate energy imbalance in one multilevel PWM cycle. A drawback is the very sophisticated predictive control. The principle has been presented only for a small number of modules.

The idea of using a quasi two-level operation of multilevel inverters has been introduced in [6] for diode-clamped inverters to ease capacitor voltage control. It has gained interest to reduce

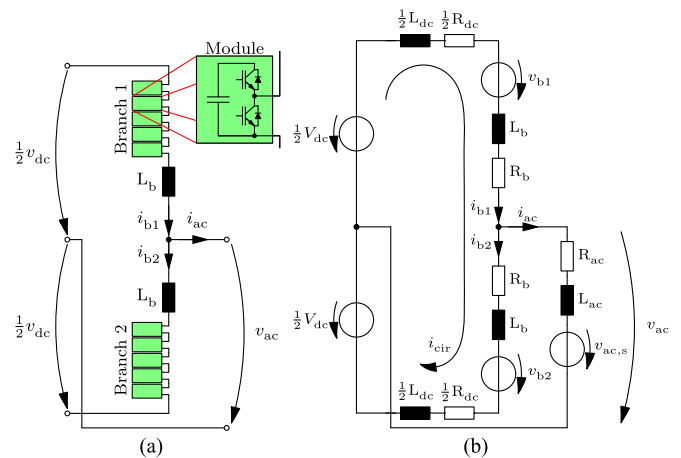


Fig. 1. MMC phase leg and equivalent circuit. (a) Topology schematic. (b) Equivalent electrical circuit.

the capacitor requirement in MMC based dc/dc converters [7] where a medium frequency voltage is used to feed a transformer. For the same application, a PWM mode has also been proposed in [8] in order to achieve a wide voltage operation and arm voltage control. Here, the switching frequency is equal to the output frequency.

This letter extends the quasi two-level operation of an MMC to a triangle-carrier based PWM in order to synthesize low-frequency output waveforms, as in conventional two-level PWM voltage source inverters. Thus, the module capacitances can be widely reduced. To achieve this, a novel power-balancing method is proposed.

II. GENERALIZED PHASE LEG MODEL

The generic building block of MMC is a phase leg as shown in Fig. 1(a). A phase leg is divided into two branches or arms, each consisting of several half-bridge modules and a branch inductor [see Fig. 1(a)]. At the converter input, a center-tapped dc voltage source is assumed. The output ac load is assumed to be inductive. The electrical equivalent circuit is shown in Fig. 1(b). The voltage sources v_{b1} and v_{b2} represent the branch voltages that can be controlled by switching the modules accordingly.

The power of the branch voltage sources (called branch power) is important. It has to be zero in average (if losses are neglected). In a conventional MMC, it has a strong positive and negative fluctuation. This is because the branch voltage and branch current have a dc component and relatively low-frequency

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The authors are with the Institute for Drive Systems and Power Electronics, Leibniz Universität Hannover, Hannover 30167, Germany (e-mail: mertens@ial.uni-hannover.de; jakub.kucka@ial.uni-hannover.de).

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ac components. The integral of the branch power is the energy variation of an arm which determines the required module capacitance.

The central idea of this letter is to mimic the voltage source inverter (VSI) operation (including PWM) by the MMC topology, with the goal to minimize the module capacitance requirement.

The circulating current i_{cir} is introduced as the average of the two branch currents. It consists of a constant dc part \bar{i}_{cir} and a variable part \tilde{i}_{cir}

$$i_{\text{cir}} = \frac{1}{2}(i_{b1} + i_{b2}) = \bar{i}_{\text{cir}} + \tilde{i}_{\text{cir}}. \quad (1)$$

The output current can also be written as a linear combination of the branch currents

$$i_{\text{ac}} = i_{b1} - i_{b2}. \quad (2)$$

In the standard operation of dc to three-phase ac MMC, the variable part of the circulating current \tilde{i}_{cir} is usually controlled to zero (only a small part is used for branch energy differences caused by asymmetries in the whole system); the dc parts \bar{i}_{cir} form a constant dc current. The output current is then split symmetrically between both branches. The complete control of MMC was explained in detail in [9] and [10].

III. QUASI TWO-LEVEL PWM OPERATION OF MMC

A simple quasi two-level operation of an MMC for a dc/dc converter was already described in [7]. The authors also made use of the idea to limit the branch power to short voltage (and current) transition times. The balancing of energy between branches is possible there because a high frequency ac output current is generated to feed a transformer. This can be used for the energy balancing without additional means.

In this paper, the new idea of combining the quasi two-level operation with a triangle-carrier based PWM is presented. Therefore, a new means of energy balancing is also needed.

The operation can be explained by the idealized curves plotted for the converter in Fig. 1(a) over two PWM cycles in Fig. 2. The output voltage reference value is synthesized using PWM at the branch voltages v_{b1} and v_{b2} (black lines in the plots). To limit the maximal rising and falling rate of the output voltage, the modules are switched delayed to each other, resulting in the stair waveform. The output filter value L_{ac} is chosen high enough to suppress the ripple of the output current. The circulating current i_{cir} is controlled to set the branch currents i_{b1} and i_{b2} to almost zero while the according branch voltages are high, in order to minimize the branch powers p_{b1} and p_{b2} which cause the branch energy variation. Therefore, the branch energy variation results only from the commutation of the branch current and branch voltage (power peaks in the figure). This power has to be compensated in the following time when the branch voltage is high, with a small current of opposite polarity, basically resetting the voltage of the module capacitor to its set-point value. This small compensating current can be controlled at a high sampling rate using the sum of the branch voltages and basically not affecting the output voltage. As a result, energy balancing is made on a PWM cycle basis and not on an output frequency basis, again reducing the necessary amount of module capacitance.

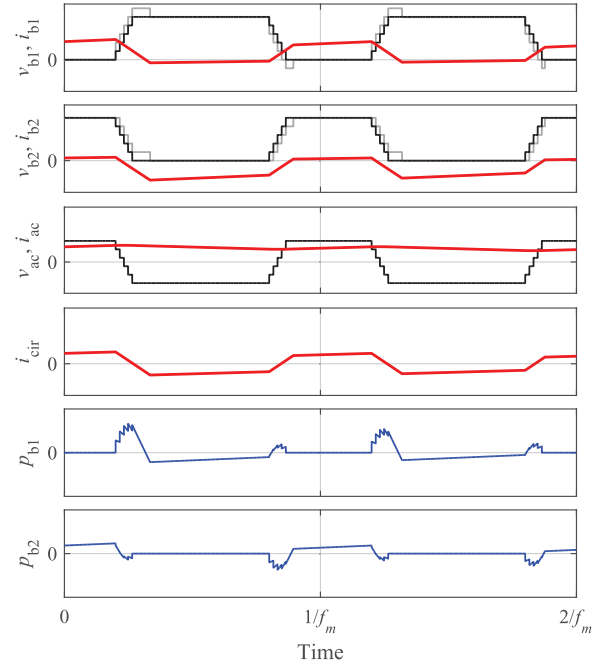


Fig. 2. Idealized curves of Quasi two-level PWM operation for two PWM cycles—operation with five modules per branch: voltages are black and gray, currents are thick red, power is blue. f_m is PWM frequency.

The rate of the circulating current rise and fall depends on the branch inductors L_b together with the parasitic inductance of the dc source L_{dc} . Their effective value $2L_b + L_{\text{dc}}$ has to be chosen low enough to enable high commutation rates. At the same time it has to be chosen high enough to suppress the circulating current ripple resulting from high-frequency PWM (HF-PWM), which is used for closed-loop control of the circulating current (as explained below). In order to achieve the fast rise and fall of the circulating current, the required voltages are inserted into both reference branch voltages. The reference branch voltages with the inserted part due to $d\tilde{i}_{\text{cir}}/dt$ are plotted in gray in Fig. 2.

In Fig. 2, it is visible that the gray branch reference voltage is partly below zero, or eventually higher than the maximum available voltage. As these voltages cannot be synthesized by the branches, the reference voltage signals need to be clipped, which leads to a distortion of the output voltage (causing a small voltage error similar to the dead-time effect).

As mentioned, for the control of the compensating current, an additional high-frequency PWM with a modulation frequency much higher than that of the output PWM is applied. The additional pulses are not displayed in Fig. 2 but they will be seen in the next section. To reduce the additional switching losses, the HF-PWM is only applied during the positive pulse of branch voltage, when the branch current is very small. For the rest of the PWM cycle, the branch current is high but the branch voltage is kept at zero, so the branch power is also zero, and no switching occurs in the modules. Therefore, the HF-PWM only has a small impact on the overall converter efficiency.

IV. CONTROL PRINCIPLE AND SIMULATION

The feasibility of the novel operation mode has been verified by simulation. A dc to ac converter consisting of one phase

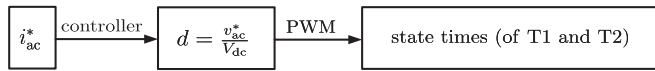


Fig. 3. Output current control scheme (outer loop).

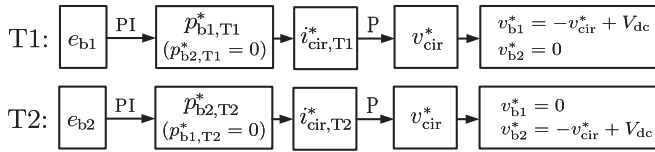
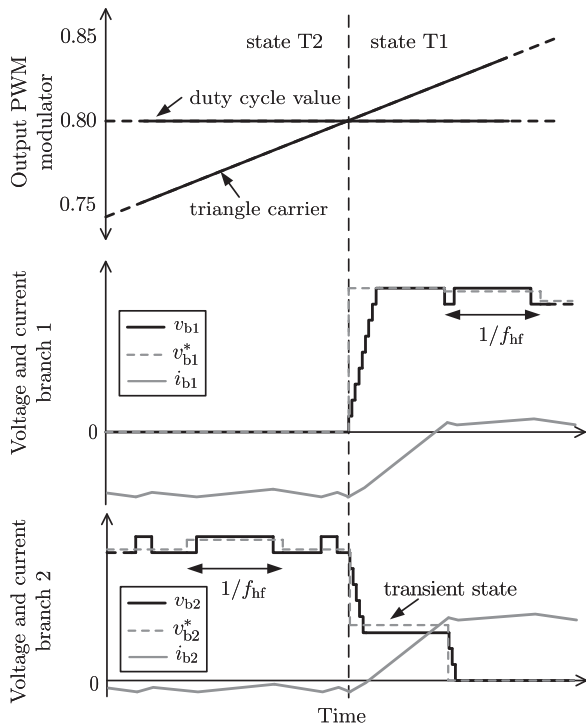


Fig. 4. Branch energy control scheme (inner loop).


 Fig. 5. Modulation principle, f_{hf} is the HF-PWM frequency.

leg as shown in Fig. 1 is controlled using cascaded controllers. There is an outer control loop with a sampling rate equal to the PWM frequency f_m (1 kHz in the example) and an inner loop which is running at the HF-PWM frequency f_{hf} (40 kHz).

The tasks performed in each of the loops are as follows. The slower, outer loop is very similar to a conventional two-level VSI, Fig. 3. It performs the output current control, resulting in the output voltage setpoint. From this, the PWM modulator calculates the output two-level PWM switching times according to a triangle carrier comparison (see also Fig. 5, top waveform). The resulting switching state times (of state T1 and T2) are forwarded to the inner control loop. In state T1, the output voltage v_{ac} is supposed to be equal to $-V_{dc}/2$ ($v_{b1} = V_{dc}$, $v_{b2} = 0$). In state T2, v_{ac} should be $+V_{dc}/2$ and thus, $v_{b1} = 0$, $v_{b2} = V_{dc}$.

The faster inner control loop performs the control of the circulating current which is responsible for the energy balancing.

Its control is explained with Fig. 4 together with Fig. 5. An overview of a complete period of the output frequency is given in Fig. 6

The circulating current is governed by the sum of the two branch voltages. Therefore, the required difference v_{cir}^* between $(v_{b1} + v_{b2})$ and V_{dc} can be added to either of the two branch voltages, whichever is appropriate.

At the beginning of Fig. 5, state T2 is active. Here, v_{b1} is zero but it is carrying the full negative load current, while v_{b2} is in the range of V_{dc} , but only a very small branch current is flowing here for energy balancing. This current is controlled in the inner control loop by adjusting v_{b2} with a HF-PWM.

When the outer control loop requests to switch to state T1 (the output PWM carrier signal becoming equal to the duty cycle setpoint, see Fig. 5), the voltage transients are initiated. The modules are switched one by one. Also, the circulating current has to be changed, so that the complete output current is flowing through branch 2 afterward. This requires a fast di/dt and a rather large voltage across the branch and dc-link inductances. This voltage is accommodated, in contrary to the rest of the time, by splitting it between the both branch-voltage setpoints. In Fig. 5, the resulting setpoint of the voltage at branch 1 is limited by the maximum number of modules. The voltage at branch 2 during state T1 is not changed in HF-PWM mode in order to avoid unnecessary switching at high current. Once the requested value of the circulating current is reached, v_{b2} is reduced to zero. The closed-loop control of i_{cir} is performed now only by a HF-PWM of v_{b1} . Note that the current in branch 1 is very low at this time, and therefore the switching losses due to HF-PWM are very low.

Obviously, the circulating current can transfer energy only to one branch at a time (the branch power at the other branch is zero, all module capacitors are disconnected there). As a result, the operation of the inner control loop has to be separated for state T1 and T2. In state T1, the branch energy e_{b1} is controlled by a proportional-integral (PI) controller, and in T2, e_{b2} is controlled (see Fig. 4).

The reference branch power $p_{b1,T1}^*$ (or $p_{b2,T2}^*$) obtained from the branch energy PI controller determines the set-point value of the circulating current $i_{cir,T1}^*$ ($i_{cir,T2}^*$). The circulating current is then controlled with a P controller, resulting in a reference voltage v_{cir}^* which is added to the nonzero branch voltage.

To realize the required branch voltages, a modified modulation from [11] with $\downarrow\uparrow\downarrow$ sequence for HF-PWM generation is used.

Also, the dv/dt limitation is introduced by the branch voltage modulators, where the minimum time period is inserted between the module switching instants.

The internal energy balancing between the capacitors in a branch is based on a capacitor voltage sorting algorithm. The modules for the switching instants are selected from those currently available according to the module capacitor voltage and the branch current (e.g., if the branch current is estimated as positive, the module capacitor with lowest voltage is switched on, or the capacitor with highest voltage is switched off).

In Fig. 6, typical waveforms of the MMC quasi two-level PWM operation are plotted. Note that the current is scaled for

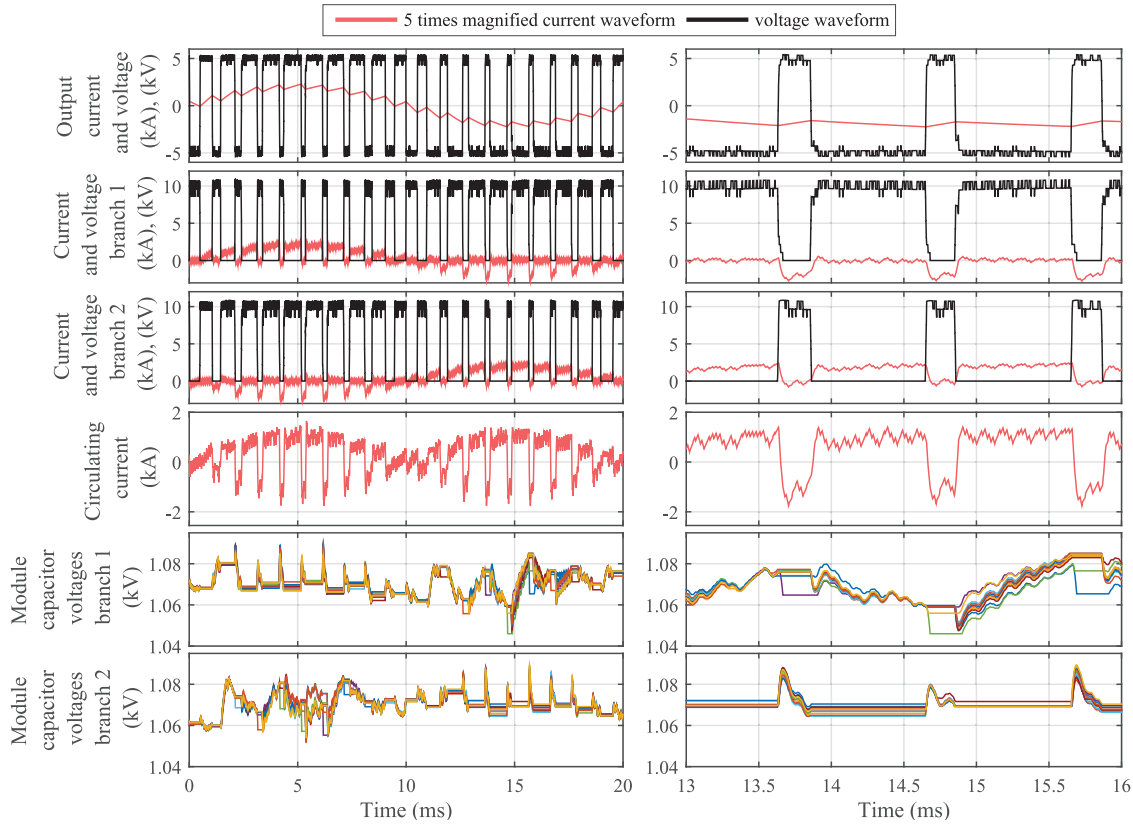


Fig. 6. Simulated waveforms of MMC with quasi two-level PWM operation: modulation index $M = 0.6$, current amplitude $\hat{i}_{ac} = 400$ A, operation frequency $f_{ac} = 50$ Hz, power factor $\cos \varphi = 1$, input voltage $V_{dc} = 10$ kV, number of modules per branch $n_{mod} = 10$, PWM frequency $f_m = 1$ kHz, HF-PWM frequency $f_{hf} = 40$ kHz, branch inductance $L_b = 75$ μ H, output inductance $L_{ac} = 15$ mH, output resistance $R_{ac} = 1$ m Ω .

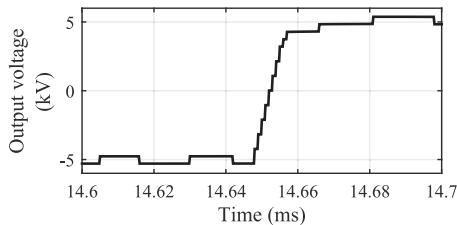


Fig. 7. Detail of rising edge of the output voltage.

better visibility. The left side shows how the output current is synthesized from the branch currents and how the branch energy variation is controlled to the minimum so that the capacitor voltages at the particular modules are kept stable within the limits. On the right side, the traces are shown in enlarged time scale, giving a better view of the commutation and its influence on the branch energies. Also the HF-PWM pulses are visible, while the branch voltages are high. The limited dv/dt rate of output voltage is shown in detail in Fig. 7.

The quasi two-level PWM operation of MMC was compared to the standard operation of the same converter for different modulation index values, see Fig. 8. The efficiency of the converter was calculated from the losses of the semiconductor devices only. The IGBT module Infineon FF650R17IE4 was selected for both cases. In the standard MMC operation, a high effective modulation frequency is not

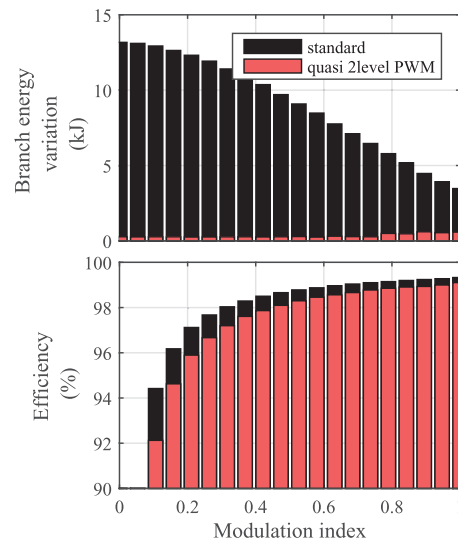


Fig. 8. Comparison of the branch energy variation and converter efficiency between the normal and quasi two-level PWM operation of MMC leg for different values of modulation index. Output frequency $f_{ac} = 50$ Hz.

required. To reduce the switching losses, 10 kHz was chosen. Therefore, the branch inductance value was increased to $L_b = 0.6$ mH.

In comparison to the standard operation, there is an enormous reduction of energy variation at the module capacitors,

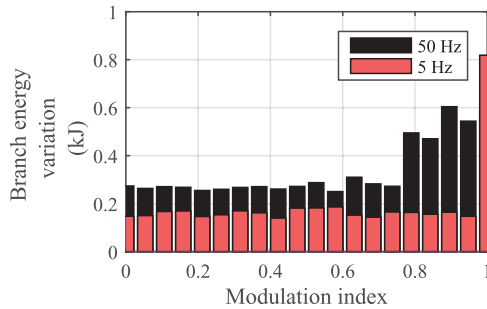


Fig. 9. Comparison of branch energy variation between quasi two-level PWM operation at 5 and 50 Hz output frequency.

as expected when the quasi two-level PWM operation approach is used. The maximum values at 50 Hz operation differ by a factor of more than 20. This means that the capacitors could be reduced in size and cost by a similar factor. The semiconductor losses are increased because higher branch currents have to be switched. The HF-PWM has only a small impact on the losses, as the switched current is very low and only one module is switching at a time. Also note that the quasi two-level PWM operation causes significantly higher output voltage distortion.

In Fig. 9 the 5 and 50 Hz quasi two-level PWM operation are compared. The lower output frequency has a positive effect on the branch energy variation. This is caused by a better performance of the PI energy controller at lower frequencies. It is also visible that the performance is worse, when the modulation index is close to one. This is caused by the decreasing width of the PWM pulses, as the converter control is not able to completely compensate the commutation energy in such a short period of time.

V. DISCUSSION AND OUTLOOK

In this paper, a novel quasi two-level PWM operation for the MMC is proposed and verified by simulation. The novel approach shows significant reduction (factor of more than 20 for 50 Hz, even higher for lower frequencies) of the branch energy variation. The lower energy variation allows selection of much smaller module capacitors, which cause a large part of the total converter costs of MMC. Of course, the multilevel property is lost.

The approach is related to a conventional two-level inverter with series connected devices but it avoids its most important disadvantages (complex gate units, extremely high dv/dt , difficult design of commutation paths), while keeping most of its advantages. The penalty is the additional power devices and signal circuitry and a more complex, but scalable control. It

inherits some of the advantages of the MMC, most important is its scalability and modularity and an easy and simple design of the series connection of the modules, because the inductance in the commutation path does not have to be minimized. In addition, a redundancy is possible without having to use press pack devices. At the same time it avoids the largest drawback of the MMC, its tremendous amount of capacitance that must be installed.

The quasi two-level PWM operation is probably most suited for applications with (variable frequency) inductive loads, such as medium and high voltage drives. In such drives, a PWM frequency of a few kilohertz can be acceptable if the additional copper and iron losses can be accommodated, whereas high dv/dt and voltage step size of direct series connection of IGBTs cannot be tolerated without additional measures.

Future research will be directed to experimental verification, to further improvement of the control, to the dimensioning of the individual converter components, and to the application of the principle to other topologies.

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